

LFAA SIGNAL PROCESSING SYSTEM PROTOTYPE TEST REPORT

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LIST OF ACRONYMS AND ABBREVIATIONS

AADC ..... Aperture Array Design and construction Consortium
AAVS..... Aperture Array Verification System
ADC..... Analog to Digital converter
ADU ..... Analog to Digital Unit board
Ad-n..... nth document in the list of Applicable Documents
AIV..... Assembly Integration and Verification
ASIC ..... Application Specific Integrated Circuit
CAD..... Computer Aided Design
CCB ..... Configuration Control Board
CDR..... Critical Design Review
CI ..... Configuration Item
COTS..... Commercial Off The Shelf
CPF ..... Central Processing Facility
CM ..... Configuration Manager
CSIRO..... Commonwealth Scientific and Industrial Research Organisation
CW..... Continuous Wave
DMS..... Document/Data Management System
ECP ..... Engineering Change Proposal
EMI ..... Electro Magnetic Interference
FoV ..... Field of View
FPGA..... Field Programmable Gate Array
FTR ..... Full Text Retrieval
HW ..... Hardware
ICD..... Interface Control Document
INFRAAUS..... Infrastructure Australia
ISO ..... International Organisation for Standardisation
LFAA ..... Low Frequency Aperture Array
LFAA-DN ..... Low Frequency Aperture Array – Data Network
LNA..... Low Noise Amplifier
LMC ..... Local monitoring and Control
LOFAR..... Low Frequency Aperture Array
MBSE ..... Model Based Systems Engineering
MCCS..... Monitor, Control and Calibration servers
MOM ..... Minutes of Meeting
MPO ..... Multi-Purpose Optic (connector)
MRI..... Master Record Index
MRO ..... Murchison Radio-astronomy Observatory
MWA ..... Murchison Widefield array
NRE..... Non-Recurring Engineering
OCR..... Optical Character Recognition
PA ..... Product Assurance
PDF ..... Portable Document Format
PDR..... Preliminary Design Review
PC ..... Project Controller
PO..... Project Officer
QA ..... Quality Assurance
RBS ..... Re-Baselining Submission

RD-N	nth document in the list of Reference Documents
RF	Radio Frequency
RFI	Radio Frequency Interference
RFoF	Radio Frequency signal over Fibre
RPF	Remote Processing Facility
SaDT	Signal and Data Transport
SDP	Signal Data Processing
SEMP	System Engineering Management Plan
SFDR	Spurious Free Dynamic Range
SKA	Square Kilometre Array
SKA-LOW	SKA low frequency part of the full telescope
SKAO	SKA Office
S/N	Signal to noise
SOW	Statement of Work
SW	Software
TCP-IP	Transmission Control Protocol – Internet Protocol
TBC	To Be Confirmed
TBD	To Be Decided
TBS	To Be Supplied
TM	Telescope Management
TPM	Tile Processor Module
TRB	Test Review Board
WBS	Work Breakdown Structure
WDM	Wavelength Division Multiplexing
WP	Work Package

1 Introduction

1.1 Purpose of the document

This document contains the Pre-construction Prototype Test Results for the SKA1 LFAA Signal Processing System (SPS) Sub-element. It presents the results of hardware, firmware, and software module prototyping to support the Technology Readiness Level (TRL) of the design detailed in the SPS Detailed Design Document [AD2]and to illustrate the reduction of the major risks for construction. More specifically, this document contains the test results of the Aperture Array Verification System 1 (AVSS-1) prototype consisting of 256 antennas, which was installed at the MRO in 2017.

1.2 Scope of the document

This document describes the prototyping test results for the SPS Sub-element <technology>. Further detail of the scope of the test is described in Section 3.

1.3 Intended Audience

This document is expected to be used by the LFAA Element Consortium Engineering and Management Team, the SKAO System Engineering Team, and the SKAO LFAA Project Manager.

1.4 Document Overview

Chapter 1 introduces the purpose, scope and intended audience for this document.
Chapter 2 lists applicable and reference documents.
Chapter 3 provides detail on the scope of the prototype.
Chapter 4 provides the procedure for the prototype testing.
Chapter 5 provides the test results from the prototyping activity.
Chapter 6 provides the test issues and related actions arising from the prototyping activity.
Chapter 7 summarises the conclusions from the prototyping activity.
Appendix A contains intellectual property declaration.

2 References

2.1 Applicable documents

The following documents are applicable to the extent stated herein. In the event of conflict between the contents of the applicable documents and this document, **the applicable documents** shall take precedence.

[AD1] SKA Request for proposal Proposals, SKA-TEL-SKO-0000020, Issue 01
[AD2] SKA LFAA Signal Processing System Detailed Design Report
[AD3] Statement of work for the study, prototyping and design on a SKA element, SKA-TEL-SKO-0000021, Issue 01
[AD4] Statement of Work for the Study, Prototyping and Preliminary Design of a SKA Advanced Instrumentation Programme Technology, SKA-TEL-SKO-0000022, Issue 01
[AD5] SKA Pre-construction Top Level WBS, SKA-TEL-SKO-0000023, Issue 01
[AD6] SKA-1 System Baseline design SKA-TEL-SKO-0000002, Issue 01
[AD7] The Square Kilometre Array Design Reference Mission, SKA-TEL-SKO-0000002, Issue 03
[AD8] SKA System Engineering Management SKA-TEL-SKO-0000024, Issue 01
[AD9] The Square Kilometre Array Intellectual Property, SKA-GOV-POL-SKOPOL-001, Issue X
[AD10] SKA1 LFAA Signal Processing System Requirement Specification
[AD11] SKA1 LFAA Requirements Specification, SKA-TEL-LFAA-0200026
[AD12] SKA1 LFAA SPS Sub-Element Requirements Specification, SKA-TEL-LFAA-0400014
[AD13] AAVS1 Requirements Specification, SKA-TEL-LFAA-0200001, Issue 1.2
[AD14] Signal processing design, SKA-TEL-LFAA-0500001, Issue 1.0
[AD15] Internal Interfaces ICD
[AD16] INFRA to LFAA ICD

2.2 Reference documents

The following documents are referenced in this document. In the event of conflict between the contents of the referenced documents and this document, **this document** shall take precedence.

[RD1] LFAA Risk Register, SKA-TEL-LFAA-0000009, Issue 12
[RD2] RX Simulation SKA-TEL-LFAA-0400014
[RD3] SKA Italian Tile Processor Board User Manual, 1.1
[RD4] AAVS1 iTPM Assembly
[RD5] AAVS1 RX automatic testing procedure
[RD6] ICRAR EMC Test Report, AAVS1 TPM Subrack
[RD7] Analog Devices Inc, The Data Conversion Handbook, Ed. Walt Kester, Newnes, 2005
[RD8] Arrants, A., Brannon, B., & Reeder, R., Understanding High Speed ADC Testing and Evaluation, AN-835 Application Note, Rev. B, Analog Devices Inc, 201
[RD9] Kester, W., Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor, MT-003 Tutorial, Rev. A, Analog Devices Inc., 2009
[RD10] ITPM ADU Board Ver. 1.0 Performance Measurement
[RD11] Naldi, G, et al., The Digital Signal Processing Platform for the Low Frequency Aperture Array: Preliminary Results on the Data Acquisition Unit, J. Astron. Instrum., 06, 1, March 2017. doi: 10.1142/S2251171716410142
[RD12] SKA RF TEST JIG, User Manual, Sanitas EG, Issue 1
[RD13] ADU Board Test Plan, Sanitas EG, Issue 1
[RD14] ADU Board Test Procedure Document, Sanitas EG, Issue 1
[RD15] iTPM Firmware Architecture, Oxford, Issue 1.1
[RD16] SKA LFAA SPS Cabinet Specification Document, Sanitas EG
[RD17] Software Demonstrator Report
[RD18] SKA LFAA conceptual sub-rack design, Sanitas EG
[RD19] Detailed Thermal Study Cooling Solution for SKA, AAVID
[RD20] Clock distribution analysis, Sanitas EG
[RD21] AAVS1 Electronics Cabinet Thermal Analysis, SKA-TEL-SKO-0210002
[RD22] Preliminary Report on RFoF costs and Performance, SKA-TEL.LFAA.RE.AST-AADC-R-001
[RD23] Preliminary Design Report of the LFAA Receiver ,SKA-TEL.LFAA.RX.MGT-AADC-R-002
[RD24] Quantization noise, linearity and spectral whitening in the LFAA quantizer
[RD25] Design of performance improvements and industrial process of SKA-LFAA receiver, LEONARDO
[RD26] Technical Report SKA LFAA Reliability Study Receiver, Università di Firenze - LEONARDO
[RD27] Availability Study Receiver, Università di Firenze - LEONARDO
[RD28] Thermal stress FEM, Università di Firenze
[RD29] Report on WDM RFoF solutions, SKA-TEL-LFAA-0400022 RX-AST-R REV 01
[RD30] Wave Division Multiplex 16 links, SKA-TEL-LFAA-0400024 RX-AST-DD REV 01
[RD31] 8 WDM 1270-1330 RFoF links
[RD32] PREADU Measurements, SKA-TEL-LFAA-0400019 RX AST-R REV 01
[RD33] Memo phase stability 1550nm on Std fibre, SKA-TEL-LFAA-0400018
[RD34] Report RX Cabling, SKA-TEL-LFAA-0400021 RX-AST-R REV 01
[RD35] Field test result Fibre Optic Cable, SKA-TEL-LFAA-0400017 RX AST-R REV 01
[RD36] Field Test Result of the 11-km Buried Fibre-optic Cable at the MRO, SKA-TEL-LFAA-0800005 RX-AST-R REV01 LFAA
[RD37] Demonstrate RFoF at Target Costs over Maximum Length the Design Requires, SKA-TEL-LFAA-0400026-RX-AE-R Rev 01
[RD38] Bench RX test description

[RD39] AAVS0.5: RFI Measurements & Updates (ICRAR)
[RD40] Test Report of ADU 1.2 boards manufactured in Italy, INAF
[RD41] Test Report of ADU 1.2 boards manufactured in NL, ASTRON
[RD42] AAVS1 Lessons Learned INAF

3 Prototype Scope

3.1 SPS Technology

Main components of AAVS1 SPS technology are electronics boards for acquiring and processing RF signals coming from the low telescope antennas, and cabinets to allocate the necessary hardware to acquire, perform the calibration and send the digitized signals coming from the field to the correlator. The Last Replacement Unit (LRU) devoted to acquisition and processing of RF data is named Tile Processing Module (TPM).
Most of electronics for AAVS1 is a custom designed and this include TPM units and TPM sub-racks. COTS components for cabinet apparatus have been used, to reduce the development efforts faced by custom solutions, as well as associated risks.
AAVS1 SPS electronics are located at the CPF, inside the CSIRO-MRO Control building. 4 cabinets and 28 TPM units are installed there.
The technical requirements applicable for the development, delivery, installation, and commissioning of AAVS1 to verify the end-to-end signal path of the Low Frequency Aperture Array (LFAA) from antenna to the output of the "station" beamformer can be found in [AD13], while a preliminary description of the SPS system was provided in [AD14].

3.2 Scope of Prototype

The planned prototyping is aimed at de-risking the technology approach and encompasses designing, fabricating, and testing of hardware as well as development and testing of key functional and performance firmware and software blocks.

The key construction risks for SPS are listed below along with a description on how the prototyping activities will address them. The Risk IDs are from the original Risk Register from the AADC consortium and regards Signal Processing and Receiver. In particular, the meaning of the various columns is as follows:

Column #1	Unique ID that should not be changed once a risk is created
Column #2	Type may be Corporate, Project, or if escalated from Element(s), their reference(s)
Column #3	Open, Acknowledged or Retired
Column #4	What project objective does this event affect?
Column #5	Who is best able to understand & control this risk?
Column #6	What is it that you are working to avoid or reduce the likelihood or impact of occurring? Risks are future events that could interfere with achievement of objectives.
Column #7	What are the triggers, sources or circumstances that could act alone or together to increase the likelihood of the Risk Event occurring?
Column #8	If this Risk Event did occur, how would it impact objectives? What are the longer-term or cumulative consequences?
Column #9	What are you doing now to reduce the likelihood or impact of the event?
Column #10	How likely? "L"
Column #11	How severe? "C"
Column #12	Risk Rating – Low, Medium, High, Unrated

Table 1. Prototype SPS Technical Risks.

ID	TYPE/RELATED IDs	STATUS	OBJ	OWNER	RISK EVENT	RISK CAUSE	IMPACT/CONSEQUENCE	EXISTING MITIGATIONS	L (1-5)	C (1-5)	RISK RATING
LFAA-SP-001	Sub-system	Acknowledged	SP	KZA	RFI-conditions changes that impacts TPM	If changes of the RFI requirements	Not fulfilling requirements	If RFI requirements will change more bits would be required which could change the processing capabilities.	1	4	***LOW***
LFAA-SP-002	Sub-system	Acknowledged	SP	KZA	Changing processing parameters will have influence on power but also on software development	Changing requirements and additional requirement for transient observations	Time delays or need for extra resources	More processing hardware and/or specific software would be required to reach the specified signal processing requirements	3	3	***MEDIUM***
LFAA-SP-003	Sub-system	Retired	SP	KZA	Bandwidth requirements change	Changing requirements	Limited time delay	Larger I/O bandwidth devices will need to be selected. Define mitigation process in case of requirement change.	0	0	***UNRATED***
LFAA-SP-004	Sub-System	Retired	SP	KZA	Number of chains on each processing board do not fit			Re-design board with fewer chains	0	0	***UNRATED***
LFAA-SP-005	Sub-system	Retired	SP	KZA	Too high processing density	Insufficient processing capability on the board	Redesign of the board or the rack(s)	Re-design of TPM or racks	0	0	***UNRATED***
LFAA-SP-006	Sub-system	Retired	SP	KZA	Power envelope not reached	Under estimated power consumption	Redesign and optimize power consumption	Re-design board with low power devices	0	0	***UNRATED***
LFAA-SP-008	Sub-system	Retired	SP	KZA	Thermal management	Large dissipation and / or less cooling power	Damaged boards/ lower reliability	Re-design of TPM or redesign of the rack cooling	0	0	***UNRATED***
LFAA-SP-009	Sub-system	Retired	SP	KZA	Still insufficient design	Interface issue of boards with rack	Redesign rack or board	Re-design of rack	0	0	***UNRATED***

ID	TYPE/RELATED IDs	STATUS	OBJ	OWNER	RISK EVENT	RISK CAUSE	IMPACT/CONSEQUENCE	EXISTING MITIGATIONS	L (1-5)	C (1-5)	RISK RATING
LFAA-SP-010	Sub-system	Retired	SP	KZA	Inrush current of a rack is to high	Filtering/ EMC protection / Component choice	Redesign and optimize inrush current	Re-design sub rack	0	0	***UNRATED***
LFAA-SP-013	Sub-system	Acknowledged	SP	KZA	Interference on other channels	Cross talk between signal channels	Re-design	Testing on prototype executed -> First estimations showed a high independency of 2 channels	0	0	***UNRATED***
LFAA-SP-014	Sub-system	Acknowledged	SP	KZA	Non linearity of ADCs	ADC performance differs from the specification giving linearity issues.	Delay - cost impact	Choose another ADC. Test linearity.	0	0	***UNRATED***
LFAA-SP-015	Sub-system	Acknowledged	SP	KZA	RFI in analogue signal path	Digital noise intruding onto analogue systems	Delay - Cost impact	Add grounding / shielding and /or filtering OR execute a redesign	0	0	***UNRATED***
LFAA-SP-016	Sub-system	Acknowledged	LFAA	KZA	Single Event Upset (SEU) and soft error rates of parts shall be known.	High integration of digital parts	Higher costs, low reliability	FPGA scrubbing/cleaning on the CPU will be used to detect such errors	1	3	***LOW***
LFAA-SP-017	Sub-system	Retired	LFAA	KZA	Main PSU not designed yet.	Lack of time	Ground loop, isolation, dissipation problems, cabling. Schedule daly and not reaching requirements.	COTS suppliers should be identified and used	0	0	***UNRATED***
LFAA-SP-018	Sub-system	Acknowledged	LFAA	KZA	Station Correlator not designed yet	Specs need to be defined	Lack of calibration	Existing software correlator code can be used, and calibration specs frozen. Work is currently ongoing to design the correlator.	1	4	***LOW***

ID	TYPE/RELATED IDs	STATUS	OBJ	OWNER	RISK EVENT	RISK CAUSE	IMPACT/CONSEQUENCE	EXISTING MITIGATIONS	L (1-5)	C (1-5)	RISK RATING
LFAA-SP-019	Sub-system	Open	LFAA	KZA	Transient Buffer ECP may change software, firmware as well as TPM architecture.	Specs need to be defined	Not fulfilling requirements	TPM hardware would have to be re-designed as well as firmware and software. Push to get the impacts on requirements as soon as possible defined and agreed upon.	3	4	***HIGH***
LFAA-SP-020	Sub-system	Open	LFAA	KZA	Clock distribution (need a better title that explains the risk. Talk to KZA.)	Specs need to be defined	Not fulfilling requirements. May impacts firmware, software and MCCS requirements.	Rack management board would have to be re-designed.	3	4	***HIGH***
LFAA-SP-021	Sub-system	Open	LFAA	KZA	The SDP-LFAA ICD may impact the software and TPM architecture.	Work started very late on the SDP-LFAA ICD.	Not fulfilling requirements, schedule delay.	Finish the SDP-LFAA ICD as soon as possible and investigate if any requirements of the Digital system will be impacted.	2	2	***LOW***
LFAA-RX-003	Sub-System	Retired	AAVS1	JM	The time schedule is tight to reach the desired deliverables, especially for AAVS1, with base requirements not still clear (i.e. technical and costs).			Improve the effectiveness /efficiency of the resources and the project management. Optimize the schedule in order to increase its efficiency considering outsourcing.	0	0	***UNRATED***
LFAA-RX-004	Sub-System	Retired	RX	JM	Some critical part as RFoF links requires a very reliable/quality production capacity in order to provide big quantity/reproducibility of devices with high MTBF.	Reliability studies not applied	Higher costs, low reliability	Improve the design studies taking into account this risk.	0	0	***UNRATED***
LFAA-RX-005	Element	Retired	LFAA	JM	Receiver technologies cost too much to reach the specified performances	Cost approach, reliability studies not correctly investigated	Higher costs	For PDR a cost calculation is made with detailed calculations based on vendor quotes	0	0	***UNRATED***

ID	TYPE/RELATED IDs	STATUS	OBJ	OWNER	RISK EVENT	RISK CAUSE	IMPACT/CONSEQUENCE	EXISTING MITIGATIONS	L (1-5)	C (1-5)	RISK RATING
LFAA-RX-006	Sub-System	Retired	RX	JM	Some supplier delay shipping /delivery	Acquisition strategy not good, agreement between customer and vendor not defined in principle	Schedule Delayed	Anticipate as soon as we can requests for devices. Find out alternative supplier. Sign for penalty in case of delay. Is covered by other risks.	0	0	***UNRATED***
LFAA-RX-010	Sub-System	Retired	RX	PE	The range of actual technology of RFoF is not as far as predicted and is not low cost/high performance	System analysis studies not investigated correctly	Higher costs, not possible to meet specifications, large time delays.	Comparison between most suitable technology RFoF link with a very accurate and qualify test plan. A common bench permits to compare results. Design a new cheaper alternative architecture considering short range TX-RX(i.e. repeat signal along the way).	0	0	***UNRATED***
LFAA-RX-011	Sub-System	Retired	LFAA	JM	The estimated performances are not as predicted.	Tests & Verification and validation plan inappropriate	Not possible to meet specifications	Simulations and performance very accurate tests for the most critical parts.	0	0	***UNRATED***
LFAA-RX-012	Sub-System	Retired	LFAA	JM	Some performance measures are impossible to evaluate because it is not possible to build a dedicated test bench for the whole distributed chain (i.e. stability requirement).	Tests & Verification and validation plan not including detailed enough tests	Unclear performances	Realize a very accurate test plan and exclude the requirements not measurable.	0	0	***UNRATED***
LFAA-RX-017	Sub-System	Acknowledged	RX	JM	PREADU performance affected from ADU and acquisition system	Tests & Verification and validation plan inappropriate	Higher costs, schedule delayed, not possible to meet specifications	Design accurate shielding and provide accurate EMI shielding	2	3	***MEDIUM***

ID	TYPE/RELATED IDs	STATUS	OBJ	OWNER	RISK EVENT	RISK CAUSE	IMPACT/CONSEQUENCE	EXISTING MITIGATIONS	L (1-5)	C (1-5)	RISK RATING
LFAA-RX-018	Sub-system	Retired	RX-SP	JM	Mechanical Rack assembly poorly defined -> cooling, routing, cabling, main PS, shielding		Higher costs, schedule delayed	Design a proper rack system	0	0	***UNRATED***
LFAA-RX-019	Sub-system	Retired	RX	JM	Crosstalk issues		Risk of not meeting specifications	Keep cross talk in mind during development Discuss cross talk on a regular base start testing cross talk when prototypes are available	0	0	***UNRATED***
LFAA-RX-020	Sub-system	Retired	RX	JM	IP2 and IP3 not as simulated		Risk of not meeting specifications	Measure IP2 and IP3 as soon as prototypes are available	0	0	***UNRATED***
LFAA-RX-023	Sub-system	Retired	LFAA/RX	JM	Use of WDM RFoF vs. single channel RFoF discussion could cause delays	WDM solutions is rather recent and needs to go through tests	Schedule delayed	The discussion process will be guided. WDM could reduces costs but could also add risks. Functionality / risks and costs should be well compared.	0	0	***UNRATED***

Concerning the previous table, the following explain what key are retired by various activities:

- LFAA-SP-003 - This risk can now be retired due to that the requirements have been defined.
- LFAA-SP-004 – Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-SP-005 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-SP-006 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-SP-008 – Valid only for AAVS1 (Acknowledged for LFAA)
- LFAA-SP-009 - Valid only for AAVS1 (Acknowledged for LFAA)
- LFAA-SP-010 - Valid only for AAVS1 (Acknowledged for LFAA)
- LFAA-SP-017 - Valid only for AAVS1 (Acknowledged for LFAA)
- LFAA-RX-003 – Valid only for AAVS1 (Acknowledged for LFAA)
- LFAA-RX-004 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-RX-005 - A detailed costing has been performed.
- LFAA-RX-006 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-RX-010 - Relevant studies have been done so this risk can now be retired.
- LFAA-RX-011 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-RX-012 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-RX-018 - Valid only for AAVS1 (Acknowledged for LFAA)
- LFAA-RX-019 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-RX-020 - Risk has been retired after AAVS1 the successful designed, produced and verified.
- LFAA-RX-021 - The risk has been retired due to that the tests have been performed
- LFAA-RX-022 - This risk can be retired due to that the investigation has shown that the analogue fibre is not too short.
- LFAA-RX-023 - Risk is retired since the WDM solution has been tested in the AAVS1 system and is now set to be the baseline option.

4 Test Procedure

4.1 Rationale and Strategy for Prototype

The strategy is to develop and test key mechanical, cooling, hardware, firmware, and software prototypes to establish the required TRL of 4-5. At the end of this activity there will be a low risk of failure should this technology and design be used in construction.
Section 4.2 defines what prototypes are developed and what key risks and uncertainties are retired by the various activities.

4.2 Development Schedule

In broad-brush terms development starting at the beginning of Stage 2 (post PDR) is likely to occur as follows, with all tasks commencing and executing concurrently:

1. PCB assembly design and fabrication.
2. Mechanical design and fabrication.
3. Incremental firmware development and test followed by testing on target hardware.
4. Software development and test.
5. Signal Model Generation.

According to [AD2], development in 1. proceeds from the Tile Processing Module (TPM) assembly to rack/cabinet assembly. The TPM assembly, consists of an Analog to Digital Unit (ADU) board and a Pre-ADU board.

4.2.1 AAVS1 Hardware

4.2.1.1 *Pre-ADU Board*

Pre-ADU board corresponds to the analogue receiver in front of the ADU. Every Pre-ADU hosts 8 double channel analogue receivers (i.e. 16 analogue chains). The two chains in each double channel receiver correspond to the two antenna polarizations. Two Pre-ADU boards are needed to feed all the ADU inputs (16 antennas/32 polarizations=32 receiver chains) and to compose the so called TPM [RD23]. The top view of the Pre-ADU board is visible in Figure 1.

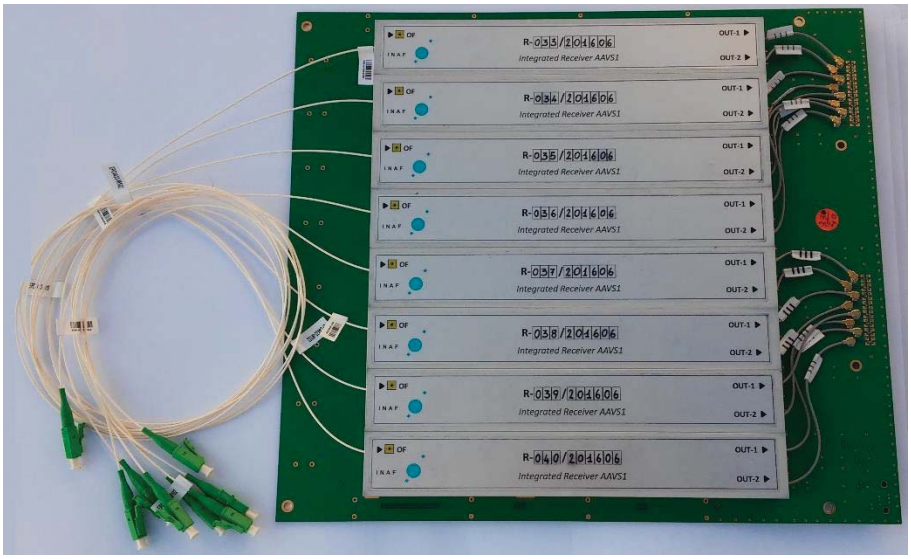


Figure 1. Pre-ADU 2.1 top view: 8 double channel analogue receivers are hosted on the same board.

The first stage of any Pre-ADU channel is an optical receiver (ORX) which converts back to the RF domain the signal transmitted through an optical fibre from the remote antenna. The current Pre-ADU version adopts WDM (Wavelength Division Multiplex) optical receivers, which paired with WDM optical RFoF (RF over fibre) transmitters at the antennas, allow to use one single fibre for both antenna polarizations [RD29].
A standard direct RF receiver (i.e. without any frequency conversion) follows the ORX. Several functions are here included in order to adapt the signal for the digital conversion: amplification, level adjustment (by means of a digital step attenuator, 31 dB range/1 dB step), band selector with a filter bank (low band, 50–375MHz, or high band, 375–650MHz) and a RF switch to close the RF input of any receiver on a 50 Ohm load for debugging procedures. The digital step attenuator and the two RF switches (band selection and 50 Ohm load) are controlled by ADU board via the SPI bus. Figure 2 shows the PCB of one double channel Pre-ADU receiver.

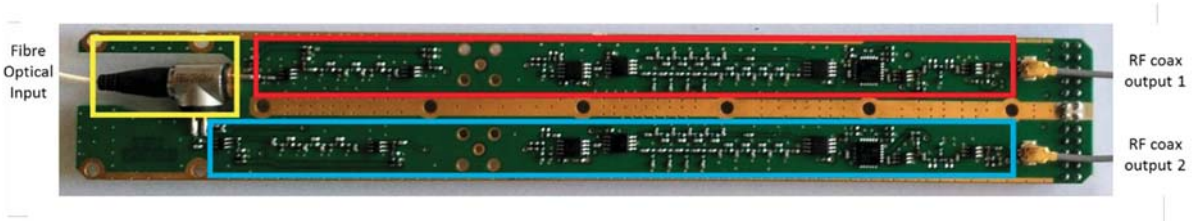


Figure 2 Pre-ADU 2.1 integrated WDM optical photodiode (yellow) and double channel RF receiver (red and

The main specifications derived from the requirements, analysis and simulation, are summarized in Table 2. For any detail please refer to [RD2].

Please note that the specifications are given for an entire RX chain because isn't possible to measure and separate the pre-ADU without the counterpart (FE) and vice versa.

During the design phase before to produce the AAVS1 version (2.1) we tested several generations of the board fine tuning the design and to mitigate the risks of the newest technologies.
The "quantum leap" has been to adopt the WDM technology (Wave Division Multiplex) instead the standard one, to carry the two polarisations in only one fibre.

For completeness they are reported here the four main generations designed and produced inside INAF laboratories.

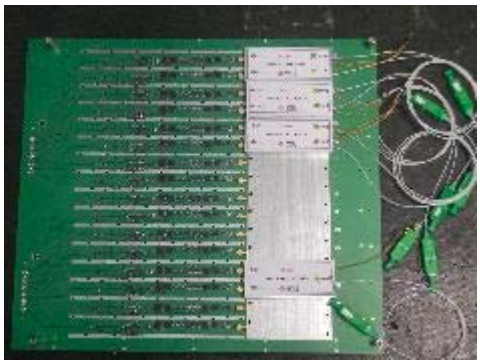


Figure 3. Pre-ADU 1.0.

First realization of 16 RF channels integrated on a single board and with separate ORX part removable as standard module (2 fibers for 2 polarizations) and WDM (1310/1550). This prototype was used to evaluate the complexity of the design and provide the first feedback for an end to end test and validation of Rx chain performances. It could mount several prototypes of ORX (ASTRON, UCAM) to evaluate the different performances of RFoF links. Optical connector used SC/APC.

Status: completed and dismissed



Figure 4. Pre-ADU 2.0.

The ORX modules are still separate to allow RX evaluation, the effect of the performances of several types RFoF links as the comparison between WDM 1310/1550 and 1270/1330). The board is still 16 RF channels with dismountable both parts ORX and RF, with a separate "carrier" board on which only the control and power supply part is mounted. Optical connector used SC/APC.

Status: completed and dismissed



Figure 5. Pre-ADU 2.1.

Some bugs from the previous version are corrected and the ORX module is integrated with the second part of RF electronics. The board is still 16 RF channels and the design is optimized only for AAVS1. Optical connector used LC/APC.

Status: Completed and installed/working on AAVS1, all data pack delivered for CDR.

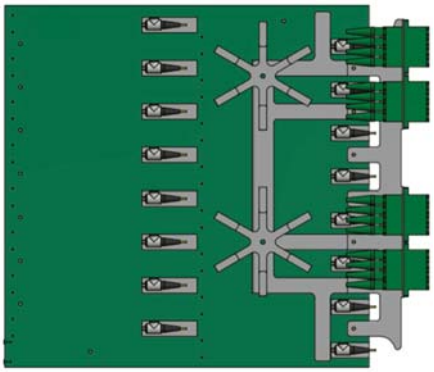


Figure 6. Pre-ADU 2.5

Engineered version for LFAA by Leonardo Finmeccanica with 32 RF channels all integrated into a single board. The goal was to understand the possibility to integrate 8 complete TPM in 1 subrack.
Optical connector used LC/APC. This version isn't described inside this document but reported in [RD25].

Status: Designed for feasibility studies for LFAA but never prototyped, data pack delivered for CDR.

Table 2. Receiver specifications.

DC specifications (at 25°C)		
Parameter	**Value**	**Notes / Conditions**
Vin FE PCA	3.5-5VDC	
Power FE PCA	<750mW	At 50°C with Vin=3.5V and without the LNA boards connected and biased.
Vin PREADU PCA	3.5VDC	
Power PREADU PCA	<1300mW	Two PREADU channels.
LNA Power Supply	3.5-5VDC >150mA	The FE module shall bias the LNA through the RF connectors.
Optical specifications		
Parameter	**Value**	**Notes / Conditions**
Nominal WDM optical wavelengths	1270nm / 1330nm	
RF requirement specifications (0-10Km of G652D SMF)		
Parameter	**Value**	**Notes**
RF band	50-650MHz	Overall frequency band
Low Band (LB)	50-375MHz	3dB cut frequency
High Band (HB)	375-650MHz	3dB cut frequency
Flatness	+/-1.5dB	Measured in the two separate sub-bands LB and HB
HP filter rejection	≥45dB	Freq≤20MHz, HP filter integrated in the FE PCA
LB filter rejection	≥45dB	Freq≥450MHz, LB filter integrated in the PREADU PCA
HB filter rejection	≥45dB	Freq≤325MHz & Freq≥750MHz, HB filter integrated in the PREADU PCA
Gain	41dB	
IRL	>12dB	Measured at both FE inputs on the overall RF band 50-650MHz.
ORL	>12dB	Measured at both ORX+RF outputs on the two sub-bands LB and HB.
NF	<22dB	
RF channels isolation	>30dB	Defined as the difference of the gains measured at the two PREADU PCA outputs with the same FE PCA input on both LB and HB bands.
OP1dB	>+17.3dBm	20dB below P1dB at nominal output power of -2.7dBm.
OIP3	>+18dBm	
OIP2	>+38dBm	
Environmental specifications		
Parameter	**Value**	**Notes**
FE PCA operational temperature	-10 ÷ +70°C	
PREADU PCA	+15 ÷ +30°C	

4.2.1.2 *ADU Board*

The ADU is the main hardware component of the TPM signal processing platform. It includes an analog part, performing high frequency acquisition and conversion of the antennas' RF signals, and a digital part, accomplishing high performance filtering and pre-processing of the acquired data.
It is a 6U board containing sixteen dual-inputs Analog to Digital Converters (ADC) and two Field Programmable Gate Array (FPGA) devices, capable of digitizing 32 RF-paths and processing digitized input signals respectively. The following devices have been selected: Xilinx Kintex UltraScale XCKU040 for the FPGA and Analog Devices AD9680 for the ADC.



Figure 7. ADU Board.

The ADU project started in 2013 with various releases of the board implemented over the last five years. The component list and board architecture have been maintained through the successive implementations. Changes concerned minor bugs, some component layout optimization needed for the soldering process input, DC-DC supply which was doubled with respect the first release (R 1.1), optimization for ADC sampling clock equalization, and firmware/software upgrade (R 1.2). In AAVS1, the most recent ADU revision is used, that is ADU 1.2.

ADU fits a 6U high and 170 mm depth standard rack mount format. While the user connectors are grouped on one side, the RF inputs are on the opposite one. Several mounting holes are present for rack mounting and to fix a heat sink.
An overview of the board mechanical layout top view is available in Figure 8.

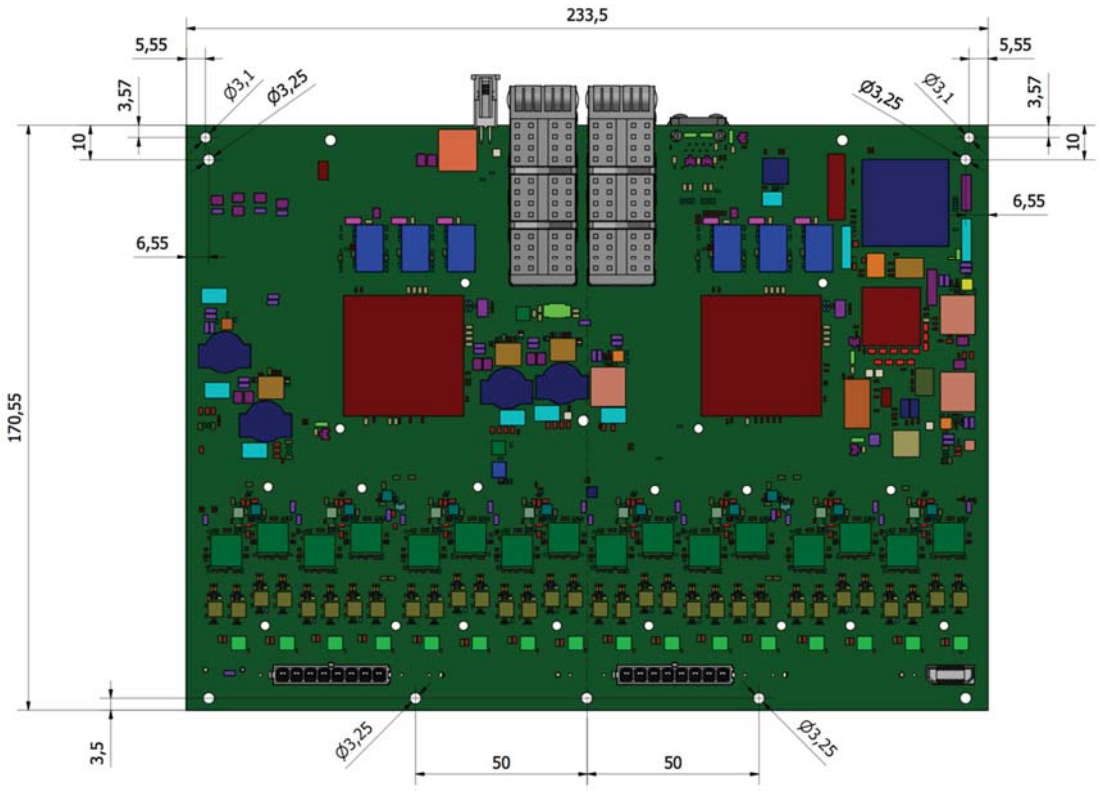


Figure 8. ADU TOP mechanical layout.

All the relevant power-dissipating devices are placed on the top side to facilitate the design of a large heat sink required for the AD devices and the two FPGAs.

The custom heat sink for passive dissipation is Figure 9.

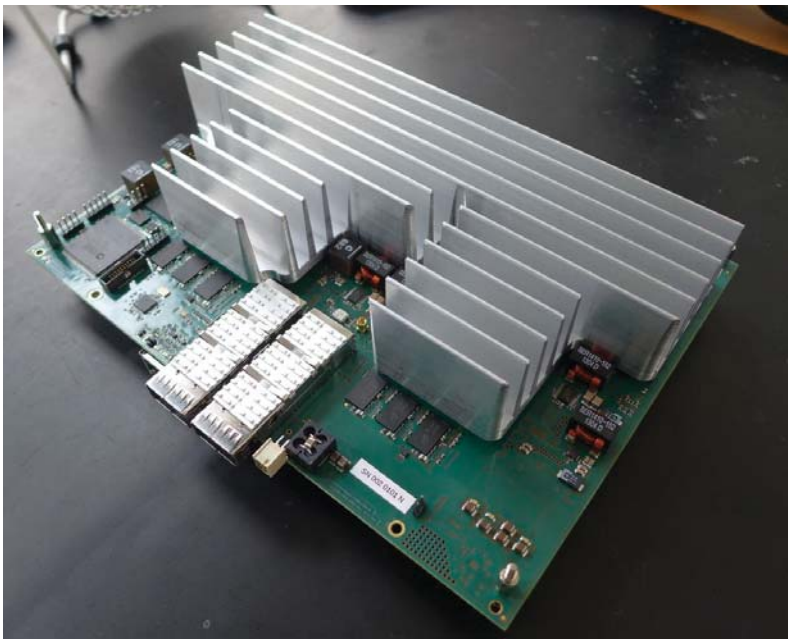


Figure 9. Heat sink, top side.

The heat sink requires adequate airflow in relation to ambient temperature and board power consumption. Main component and PCB temperature sensor available on the board shall be monitored to verify correct dissipation. Al the DC-DC converter and the AD converter are protected from internal maximum temperature.

ADU Heat sink provide also electromagnetic shielding of the input RF transformer and protect board analog area from possible damages.

A bottom side heat sink is also available for mechanical issue and to complete the transformer shielding on the RF input side.

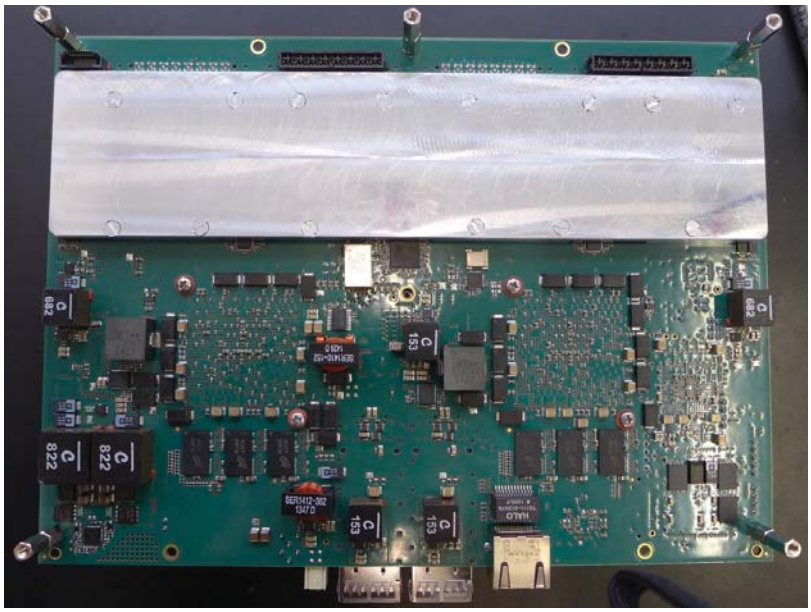


Figure 10. Heat sink, bottom side.

The following tables show the absolute maximum ratings and the recommended operating conditions for the ADU board.

Table 3. Absolute maximum ratings.

Absolute maximum ratings					
	Component	**Min**	**Max**	**Units**	**Note**
Input supply	J22	11.5	36	Volts	Max 150 Watt
PPS in	J14	5	20	mA	Forward Current
Board center temperature	U245	5	85	°C	ADC PCB max temperature
10 Mhz clock in	J1				
Front end digital I/O	J20, J21				
RF input	J15-J18				

Table 4. Recommended operating conditions.

Recommended operating conditions					
	Component	**Min**	**Max**	**Units**	**Note**
Input supply	J22	12	24	Volts	Max 125 Watt
PPS in	J14	5	16	mA	Forward Current
Board center temperature	U245	5	65	°C	Expected ADC Junction temp. 80°C
10 Mhz clock in	J1				
Front end digital I/O	J20, J21				
RF input	J15-J18				

The ADU board is organized in three areas, from left to right (Figure 11): management and power supply, FPGA and memories, analog signal interface.

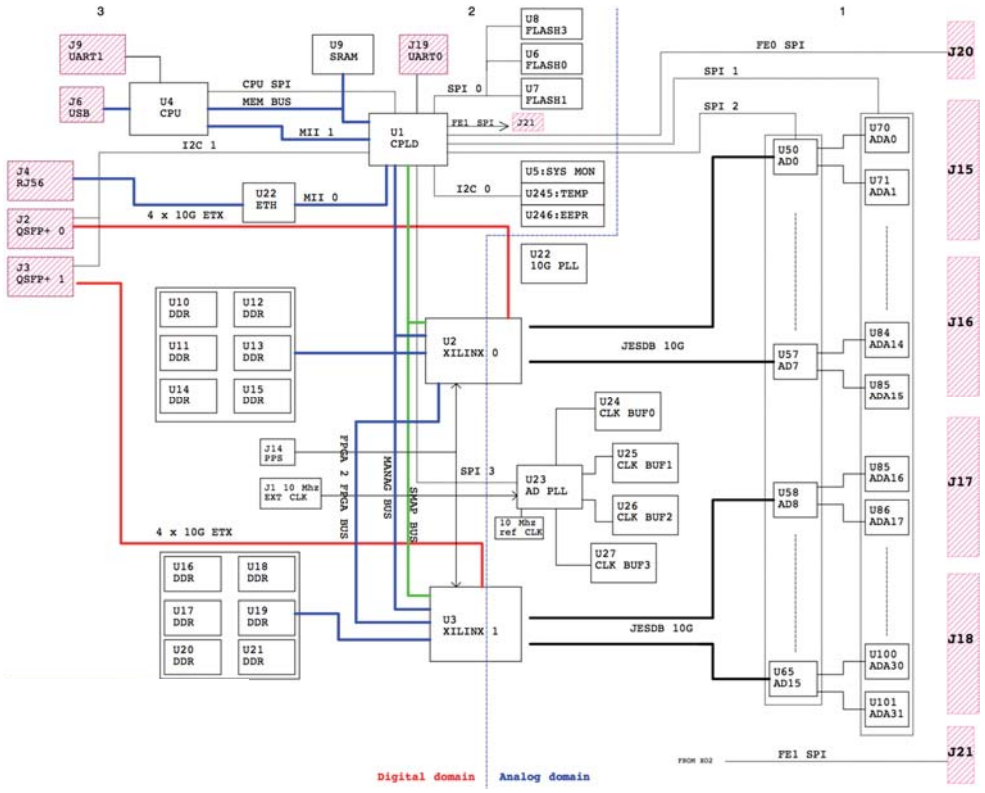


Figure 11. ADU board Block Diagram.

The organization of physical components layout into three separate areas has been adopted to obtain performance and noise isolation between DC-DC converter, digital elements and analog interface:

- The **management interface** includes the 10/100/1000 data link, the FLASH based CPLD (U1), the SYSTEM MONITOR (U5), the SPI FLASH memories (U6, U7, U8), the CPU (U4) and the CPU external SRAM (U9).
- The **FPGAs** are two identical devices (U2, U3) that provide suitable and efficient resources to implement all the main board data management and elaboration.
- The **analog section** includes the acquisition clock generation and distribution network (U23, U24, U25, U26, U27), the sixteen dual channel ADCs (U50-U65), the thirty-two analog buffers (U70-U101) and the four RF high isolation x8 input connectors (J15-J18). Two connectors (J20 and J21) provide supply and digital SPI control for a pluggable analog board for signal over-fiber connection and physical connection.

The study for the realization of the analog to digital conversion chain was previously developed in collaboration with the Analog Devices Inc. (ADI). As a result, it has been produced a dual solution using the latest ADC chip technologies (not yet available on the market): a passive matching network (without power amplifier before ADC) and an active matching network (with power amplifier before ADC).

The acronym ADA is adopted in the document to identify the Analog Devices ADA4961 which is a high performance BiCMOS RF digital gain amplifier (DGA). Having a very low IMD3 it allows converters to achieve their optimum performance with minimal limitations of the driver amplifier. It is optimized for wideband, low distortion performance up to 2 GHz. It has a gain step size of 1 dB with maximum power gain of 18 dB (15 dB of voltage gain) programmable via SPI bus.

Conversely, NO ADA board means a board that does not use such a device. ADU 1.2 boards employed in AAVS1 are NO ADA boards.

4.2.1.3 *TPM*

AAVS1 TPM is an assembly of ADU 1.2 and Pre ADU 2.1. A picture is shown in Figure 12.

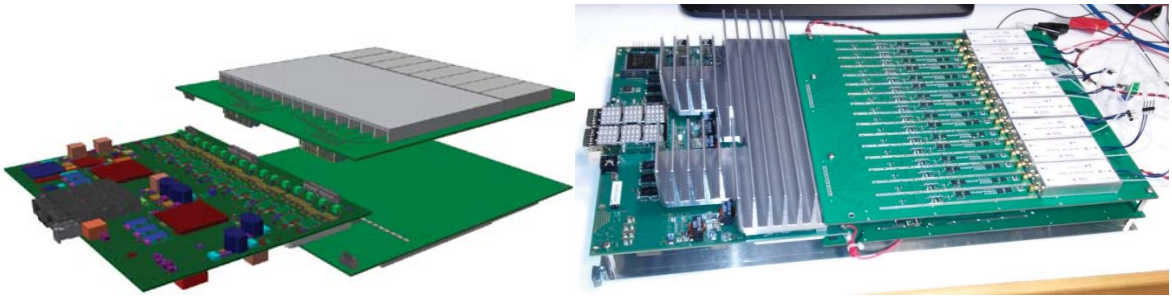


Figure 12. Exploded view drawing of TPM obtained with 3D CAD (left) and picture of fully assembled module (right).

4.2.1.4 *Rack/Cabinet*

The CPF, inside the CSIRO-MRO Control building, is the location where the AAVS1 SPS hardware has been installed.
Four cabinets are dedicated to allocating the necessary electronics to acquire, perform the calibration and send to the correlator the digitized signal coming from the field.
All cabinets need to be appropriately cabled in order to power, synchronize, manage the boards and route the data to the high-speed switches.
These cabinets are named Rack 57", "Rack, 58", "Rack59" and "Rack 60".

A commercial cabinet "Schroff Varistar LHX20", has been chosen to accommodate all the required hardware.



Figure 13. Schroff Varistar LHX20.

Following, a stack up of the four cabinets is shown from Figure 16 to Figure 19. Three of them have the same layout: 2 TPM sub-rack, References Distributor (10MHz e PPS), TPMs Main Power Supply, Power Supply Distributor, 1GB Ethernet switch and 40GB ethernet switch.
Rack 60 is equipped with a single TPM sub-rack, References Distributor (10MHz e PPS), TPM Main Power Supply, Power Supply Distributor, 1GB Ethernet switch and 40GB ethernet switch.
In this cabinet it is implemented the Main Server for controlling the complete AAVS1 backend.

TPM sub-racks are custom made while, References Distributor, TPMs Main Power Supply, Power Supply Distributor, 1GB Ethernet Switch and 40GB Ethernet Switch are “COTS” devices. In the following Table (Table 5) there are links to the manufacturer of these devices:

Table 5. “COTS” Devices: Brand, Model and link to datasheets.

Device	Brand	Datasheet
References Distributor	NI - OCTOCLOCK	CDA-2990

TPMs Main Power Supply	TDK LAMBDA	GEN 3U – 10/15kW
Power Supply Distributor	ICT Ltd..	ICT200DB-12IRC
1GB Ethernet switch	NETGEAR	S330-28X
40GB Ethernet Switch	MELLANOX	SX1012

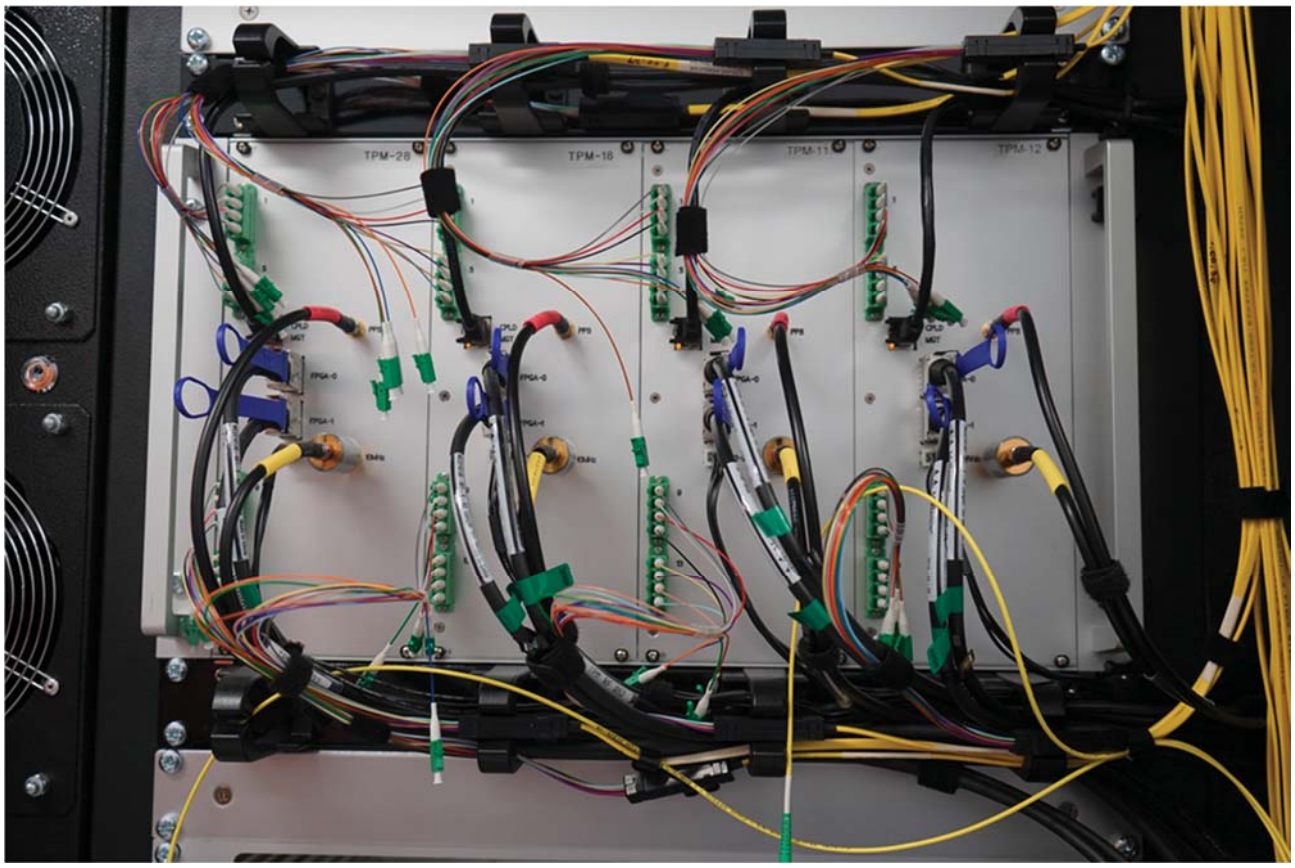


Figure 14. Close-up of a sub-rack with 4 TPM units.



Figure 15. Two AAVS1 Cabinets.

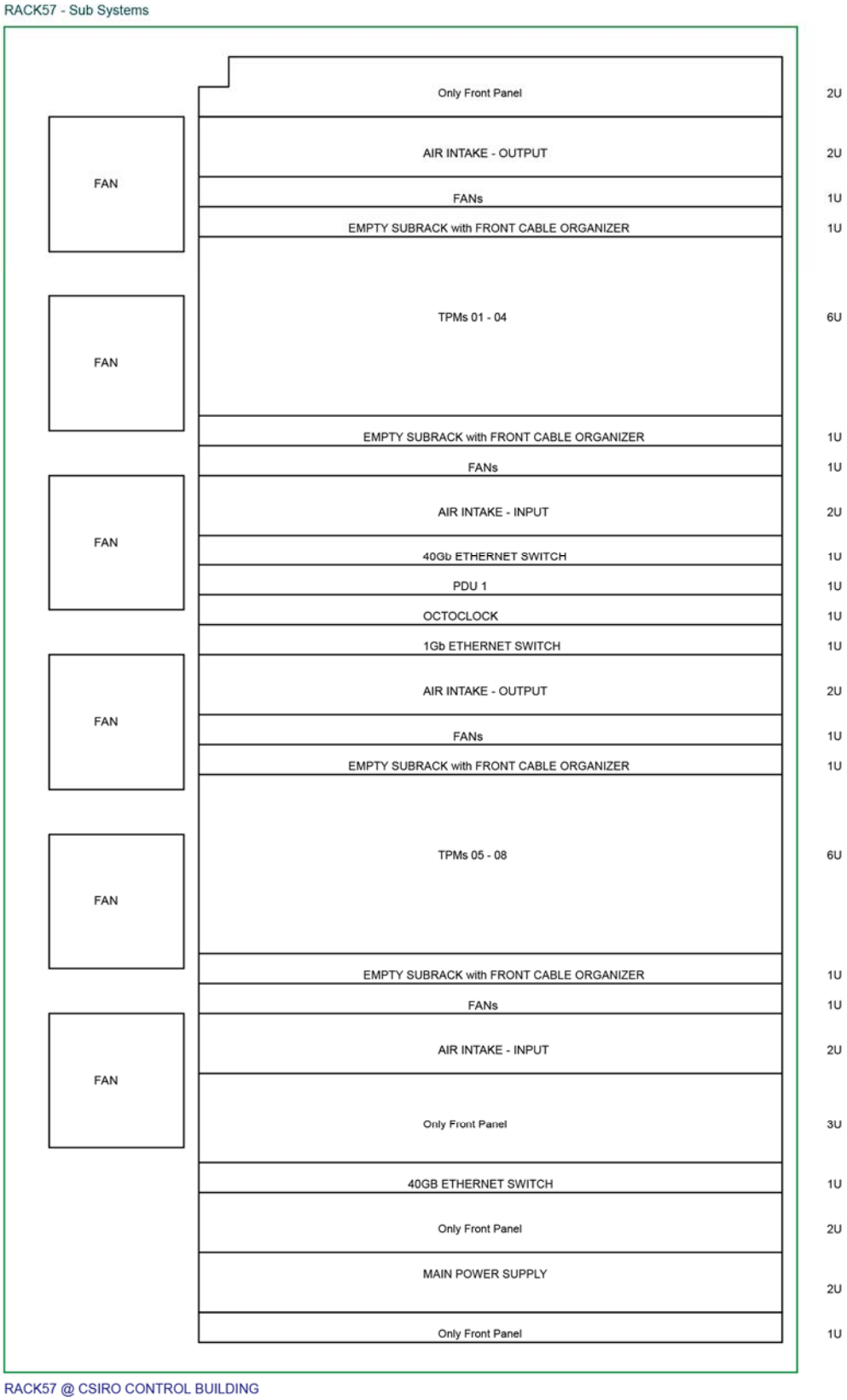


Figure 16. : Rack 57 – TPM 01 to 08.

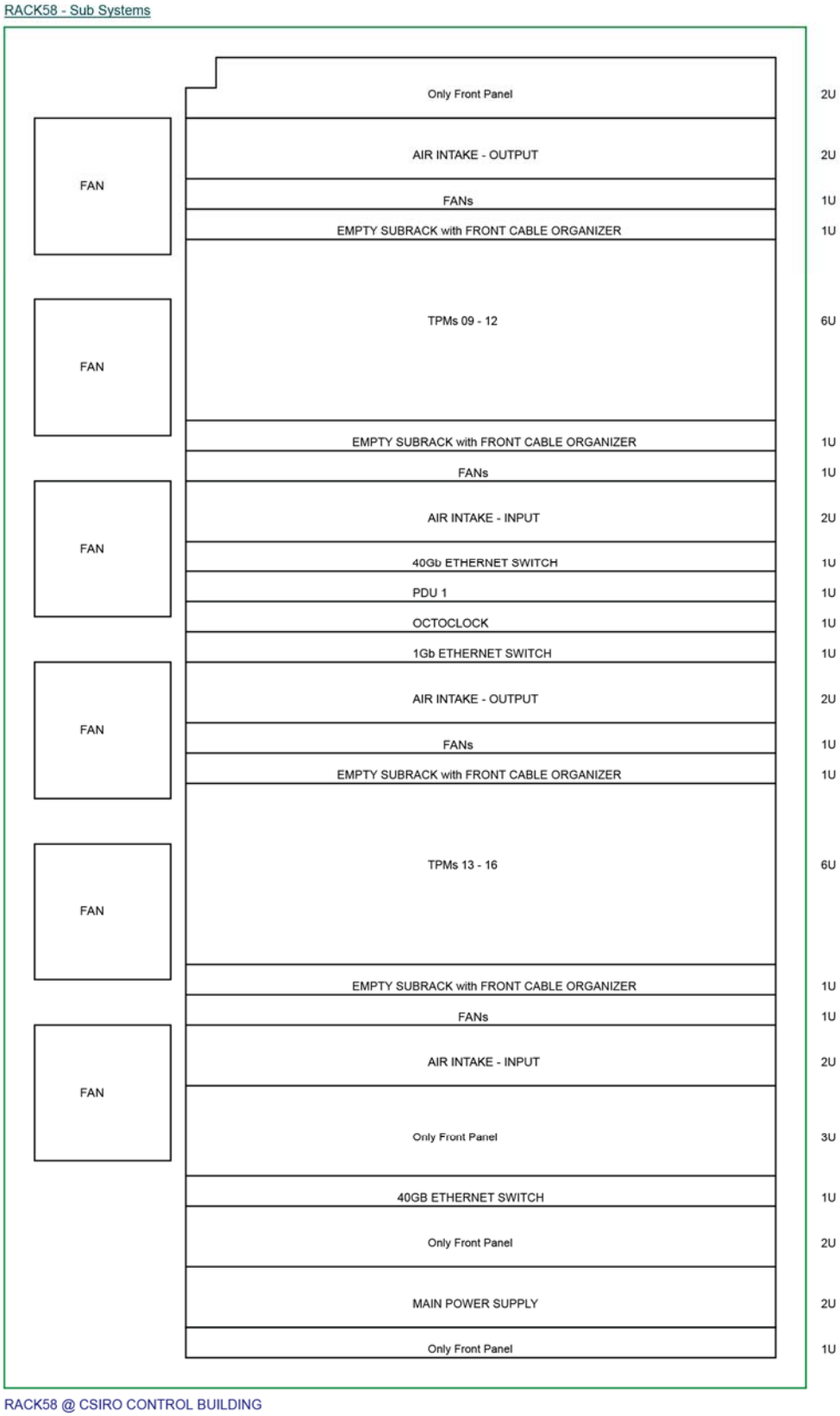


Figure 17. Rack 58 – TPM 09 to 016.

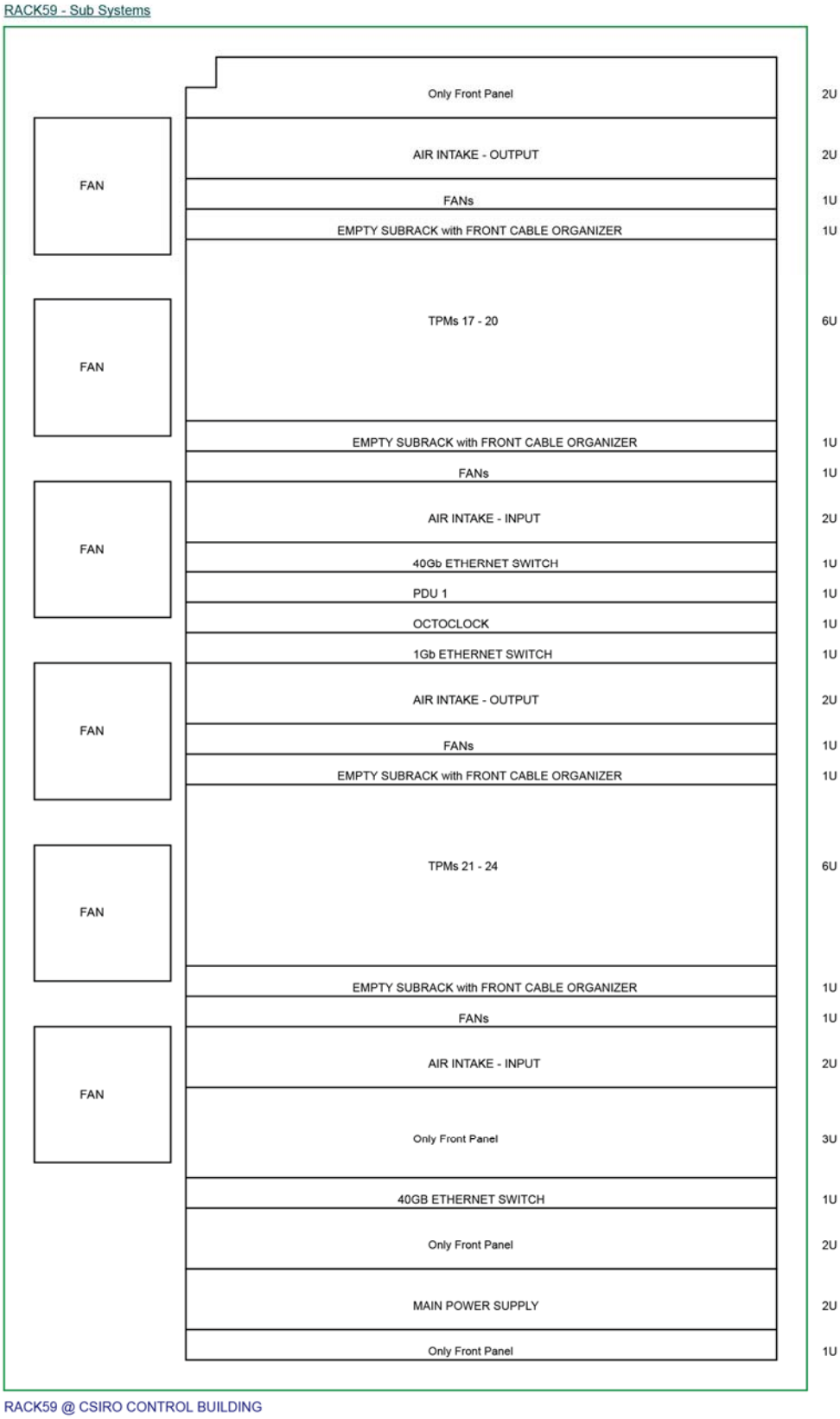


Figure 18. Rack 59 – TPM 017 to 024.

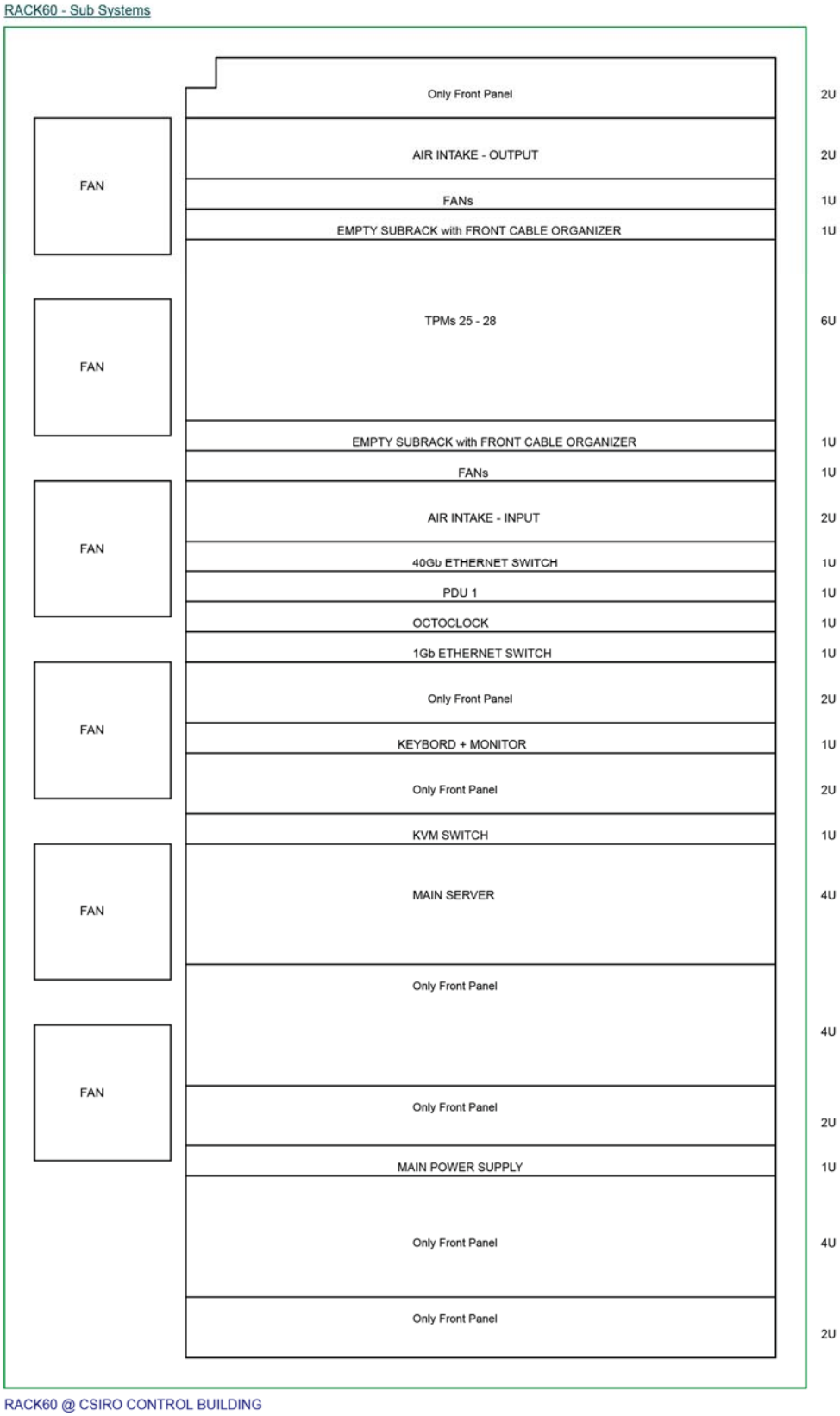


Figure 19. Rack 60 – TPM 025 to 028.

4.2.1.4.1 Cabling

Wiring is a design activity that is often overlooked.
In our specific case, the cabinet populated by the various TPMs boards inside the proper sub-rack, must be wired to bring the synchronization signals, power supply, the network for maintenance and data transportation. Inside the cabinet there are power distribution systems and clocks, as well as low and high-speed switches.

A – Main references clocks (10MHz and 1PPS), provided by external sources.
A dedicated OCTOCLOCK is used for splitting the reference input in four copies that are distributed to each cabinet.
B – Signals coming from antennas, provided by optical fiber link.
Each breakout cable coming from the splicing cabinet cable is a ribbon cable with 12 single mode fibers and LC/APC connectors.
C – The 40Gb and 1Gb Ethernet Lan.

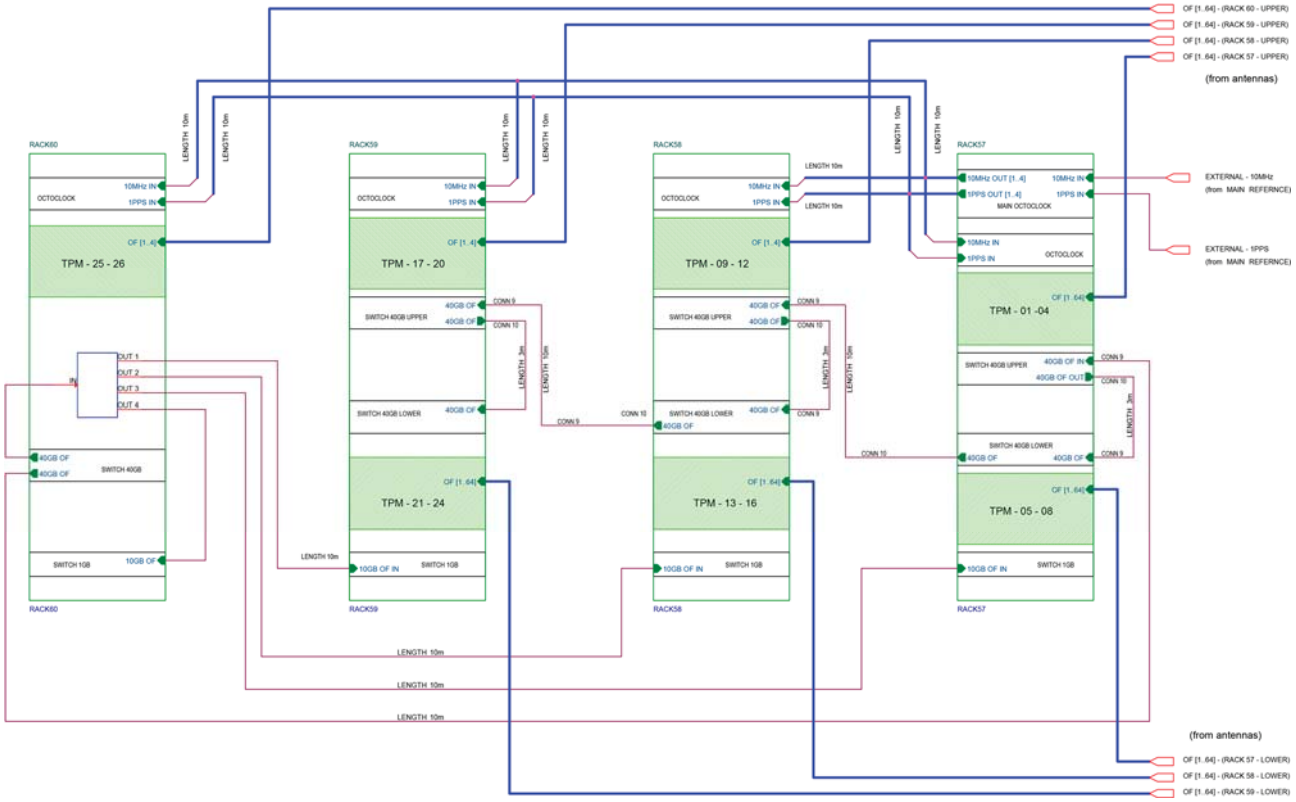


Figure 20. External reference and RF Signals distribution between cabinets.

Reference Distribution:
Both references, 10MHz and 1PPS, are provided from an external main reference to a main distributor (MAIN OCTOCLOCK) located in the back side of RACK57. From that, 3 outputs with a 10m long coaxial cable are connected to other cabinets, RACK58, RACK59, RACK60 (as shown in Figure 20) where another OCTOCLOCK distributor is installed. Thus, the outputs of this distributor, are connected to the TPMs using 1.8m long coaxial cables. For practical reasons, the distributor outputs are set using OUT1 to OUT4 for the Upper TPMs sub-rack and OUT5 to OUT8 for the lower TPMs sub-rack.

1GB and 40GB Ethernet Distribution:
From a main 40Gb Switch located in the RACK60, one of its output ports is sent to a 4-way splitter. So, 4 signals at 10Gb are generated. Each one of them, using a 10m long FO cable, is sent to the input port

of a 1Gb switch located in each cabinet. This device, using this 10Gb input signal, can generate a number of 1Gb signals that are distributed inside the cabinets using 2m long CAT5E RJ45 Ethernet cables.

Power Distribution:
Each cabinet is equipped with a remotely programmable DC power supply followed by a dual bus PDU with six independently controlled and monitored (by 1Gb Ethernet) output channels per bus. The "A bank" provides power supply to Upper TPM sub-rack and the "B-Bank" is dedicated to the Lower TPM sub-rack. In Rack57 and Rack58 suitable power cords provide power supply to TPMs. In Rack59 and Rack60 they aren't installed any power cords yet.

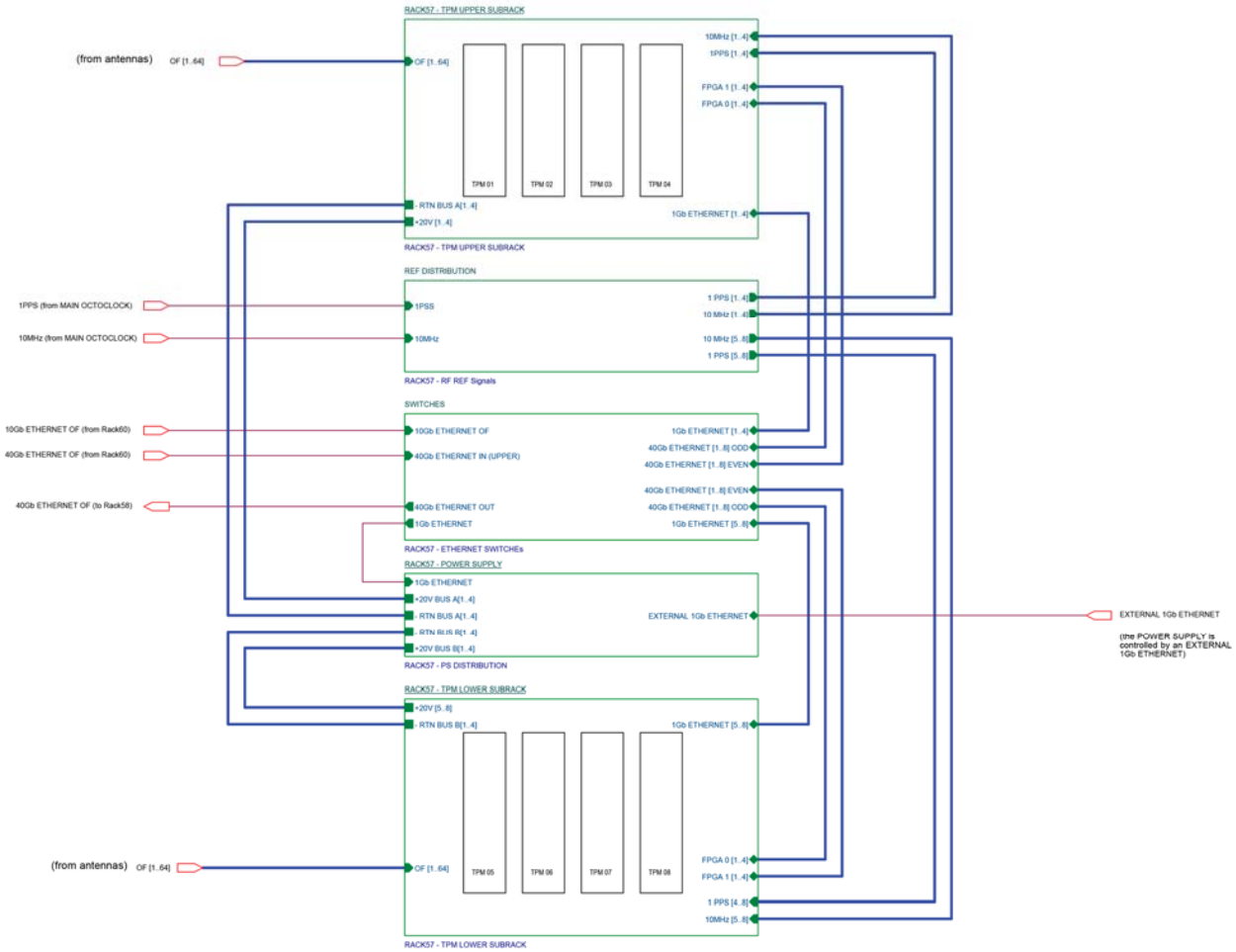


Figure 21. Rack57, Rack 58 and Rack 59 internal wiring.

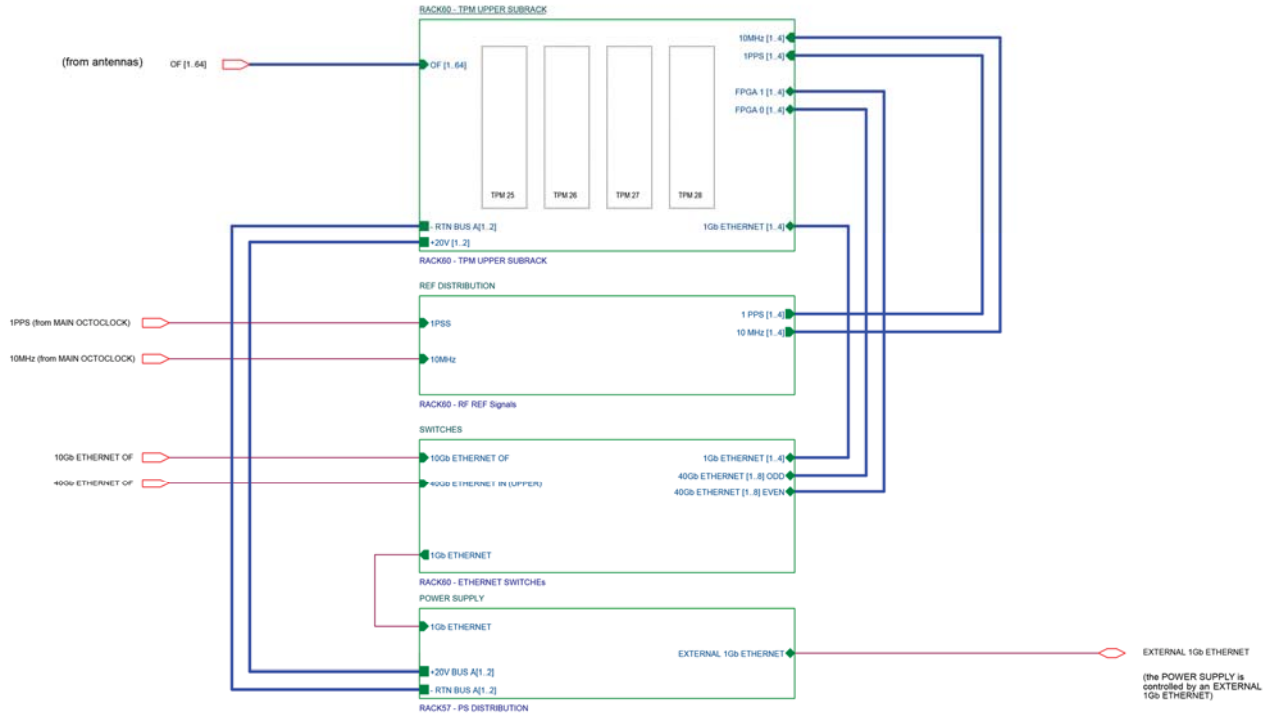


Figure 22. Rack 60 internal wiring.

The following table shows the type and the total number of cables:

Table 6. Complete Cables list for wiring AAVS1.

Q.ty	Cable type	Notes	Cable Length
52	RG223	Note: Hand-made @ Medicina Labs	1.8m
8	RG223	Note: Hand-made @ Medicina Labs	10m
52	LAN 40Gb		1m
30	LAN 1Gb		2m
26	Power Supply		Max 2m
52	OF Ribbon		----------
3	LAN 40Gb OF		3m
3	LAN 40Gb OF		10m
4	1Gb OF		10m
4	LAN 1Gb		----------

The number of cables that are necessary to completely wire all the AAVS1 cabinets system is very high. As a main consequence, it become very difficult to have a clean system cabling. For this reason, for LFAA it is strongly suggested to implement and design a different system where to minimize the cabling.

4.2.2.1 Mechanical design and fabrication

In the following, the mechanical design of the TPM, ADU and Pre-ADU boards are illustrated. The complete set of drawing is contained in [RD4].

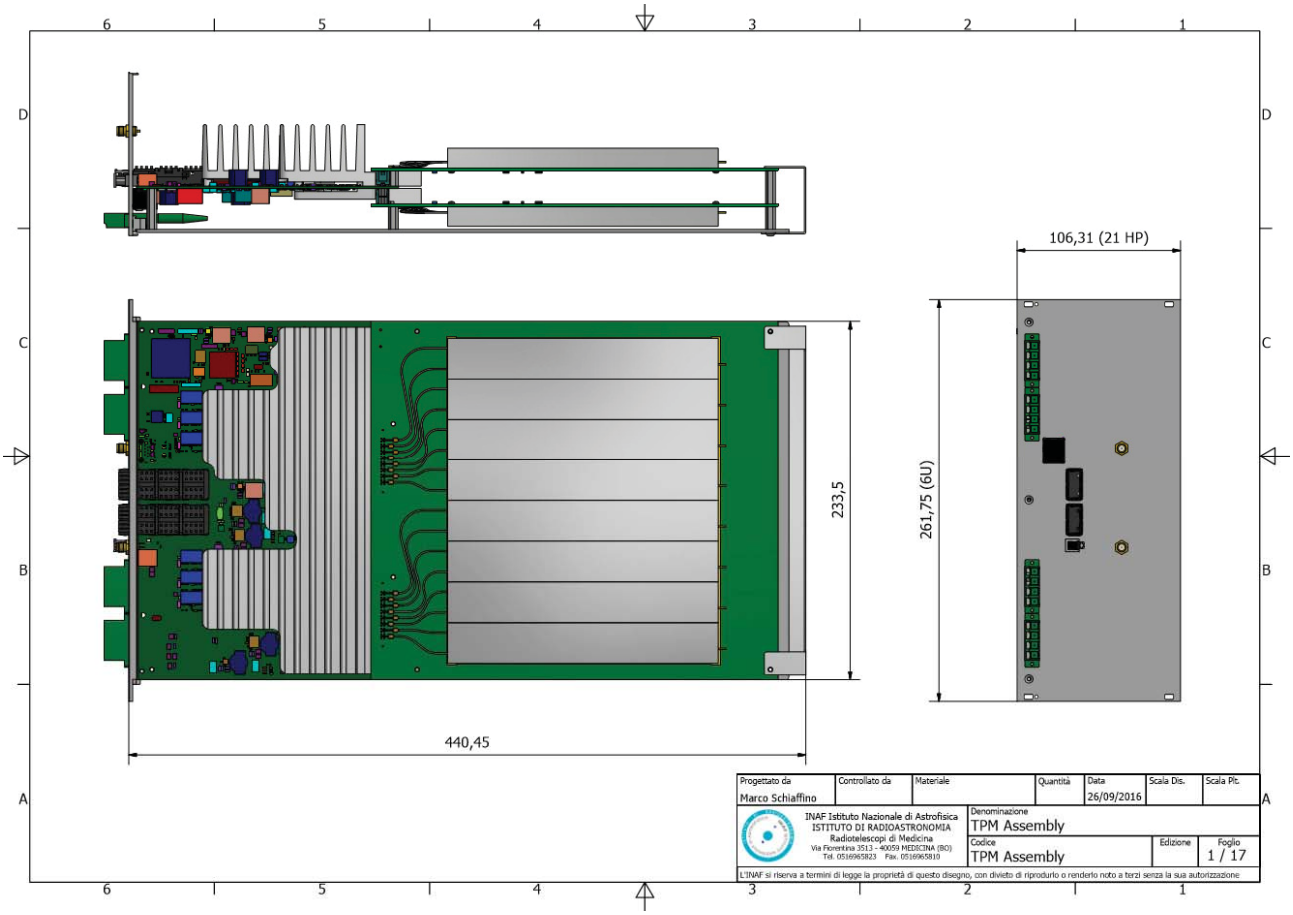


Figure 23. TPM assembly (left) and related front panel (right).

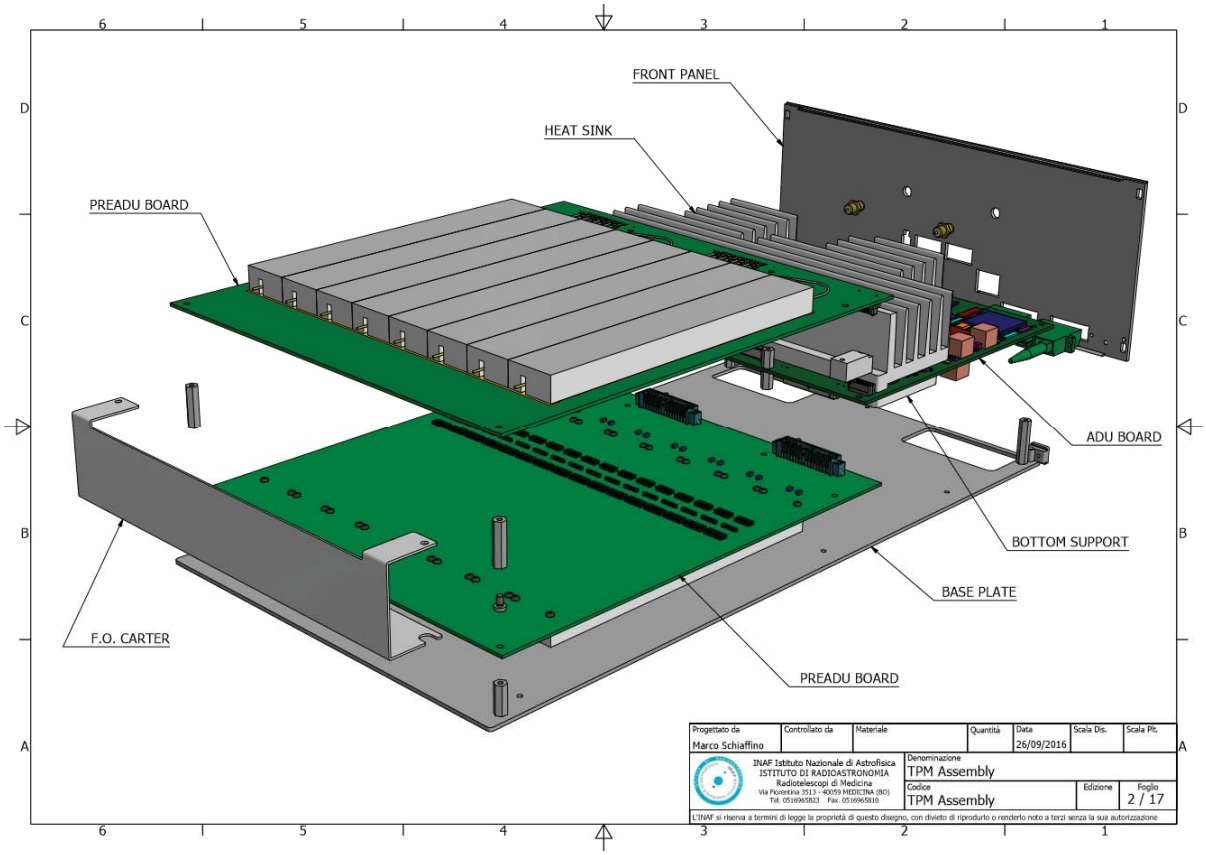


Figure 24. Exploded view of TPM assembly with parts.

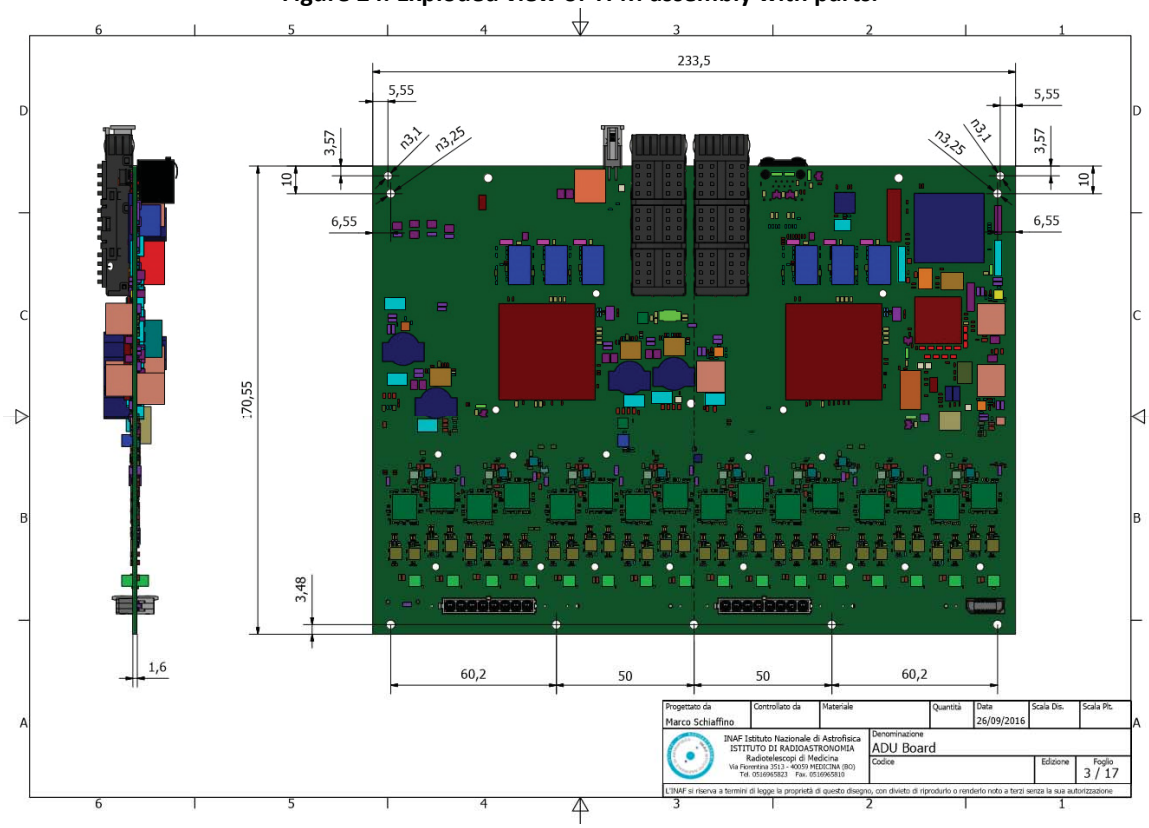


Figure 25. ADU top Layer (right) and a section with part volumes (left).

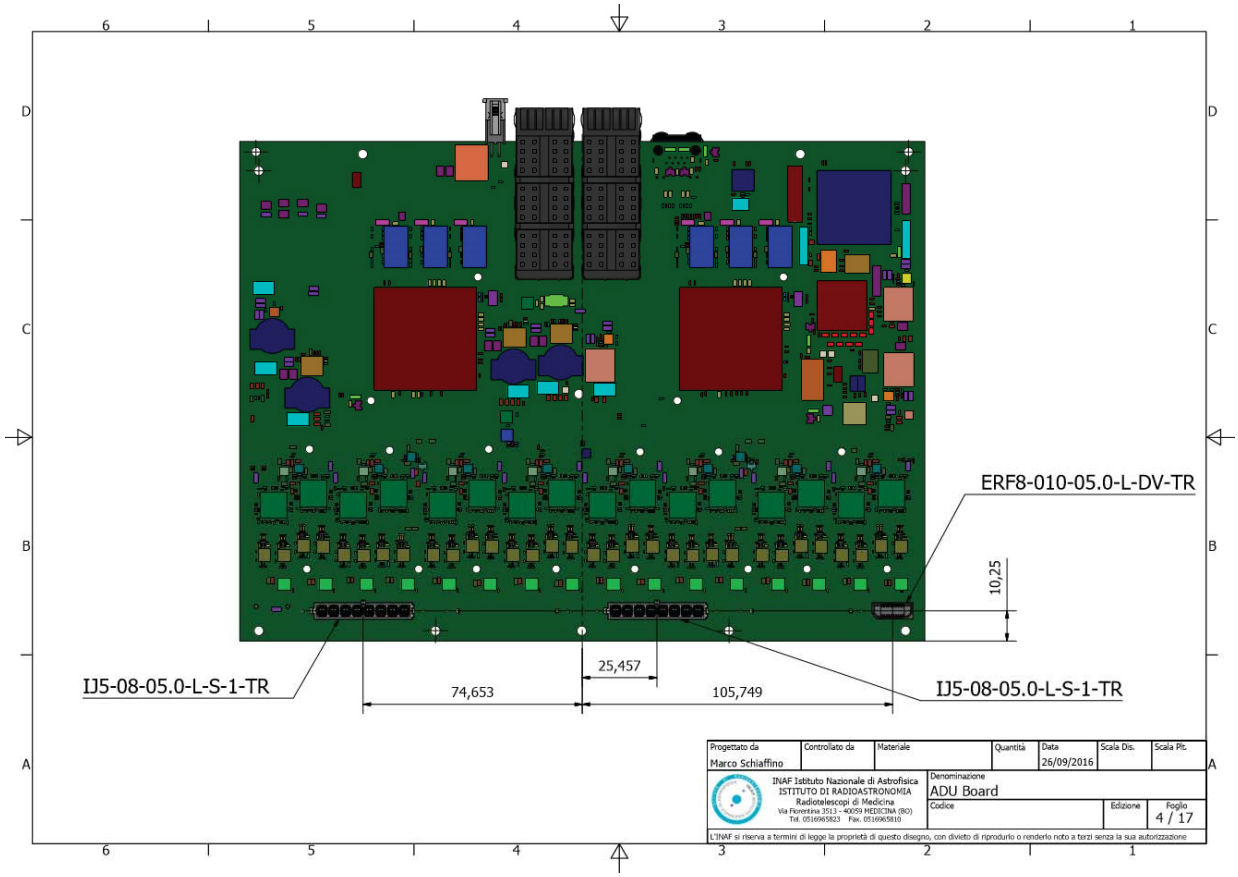


Figure 26. ADU top layer.

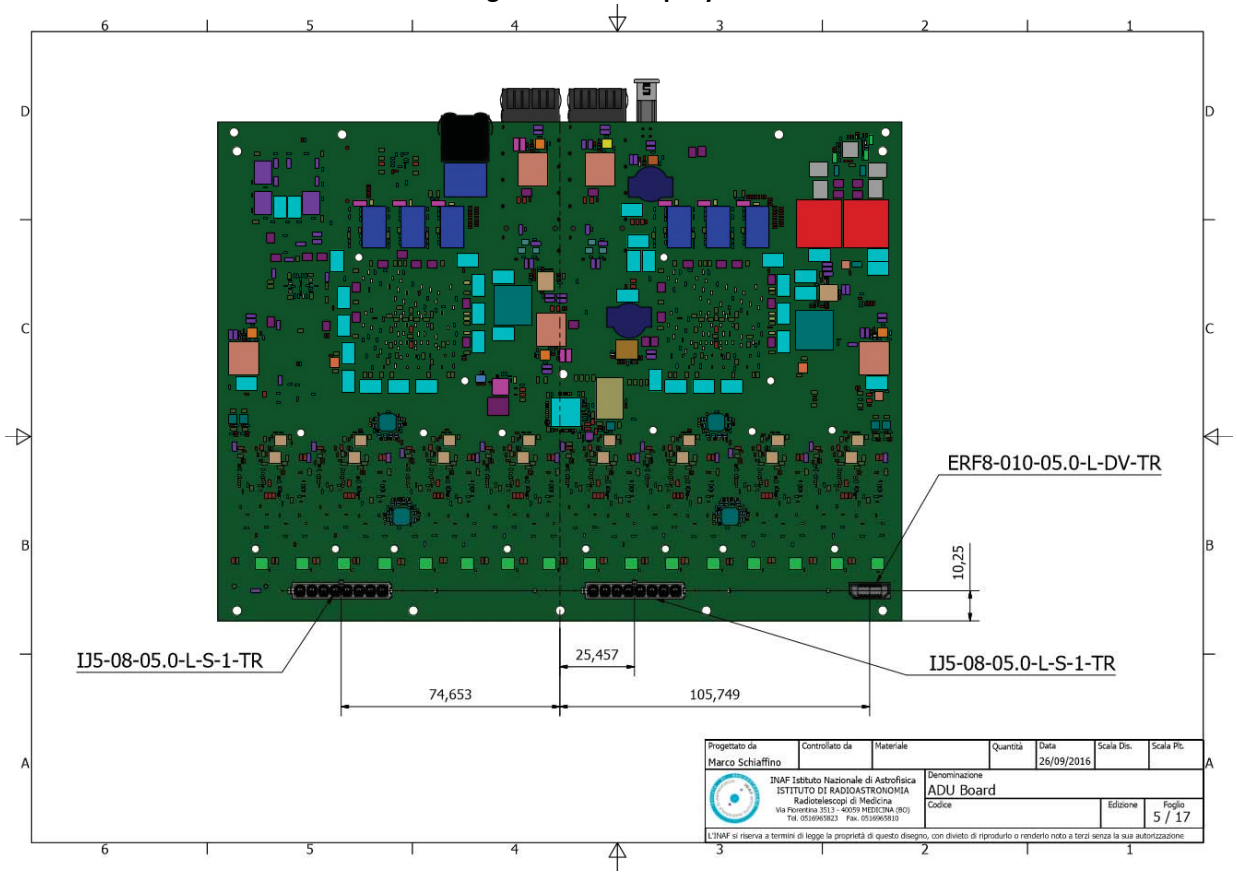


Figure 27. ADU bottom layer.

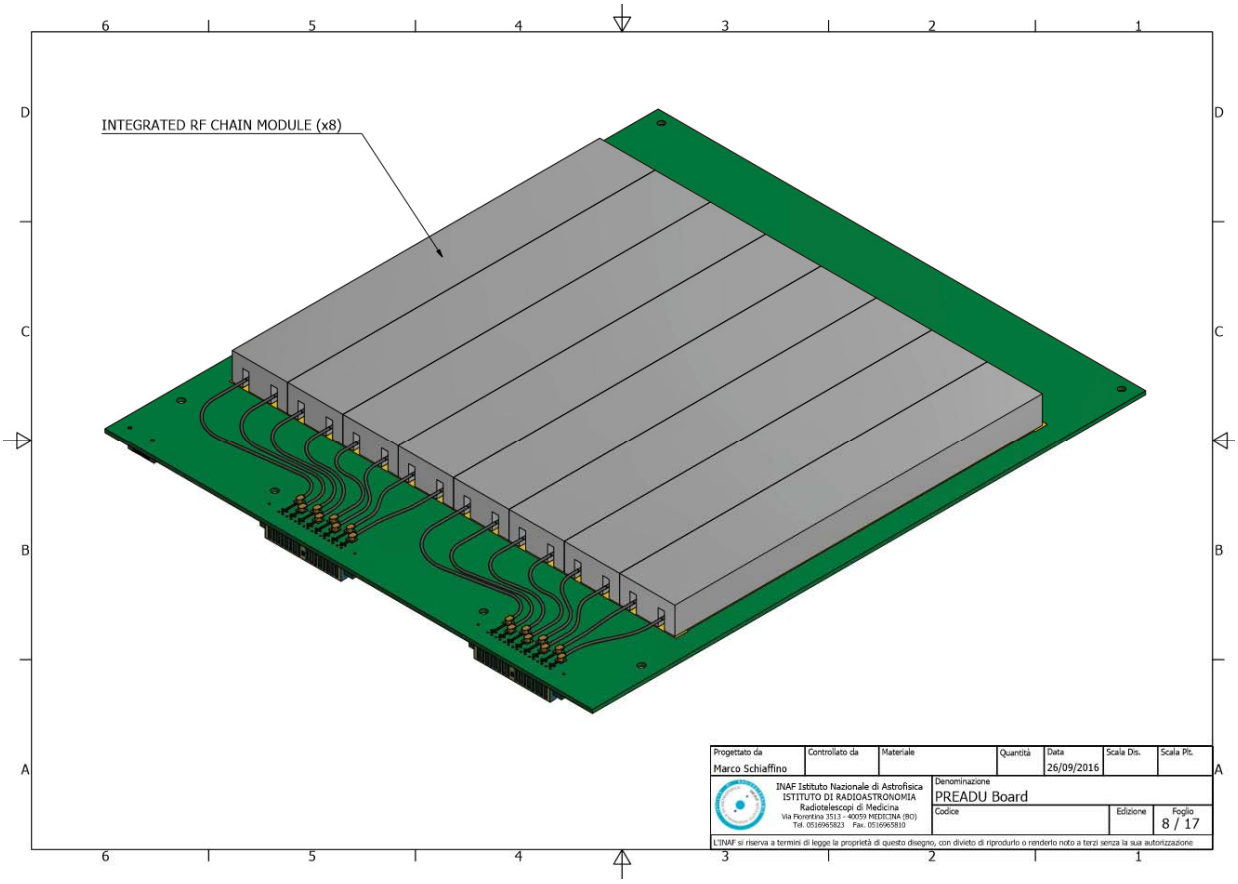


Figure 28. Pre-ADU top layer.

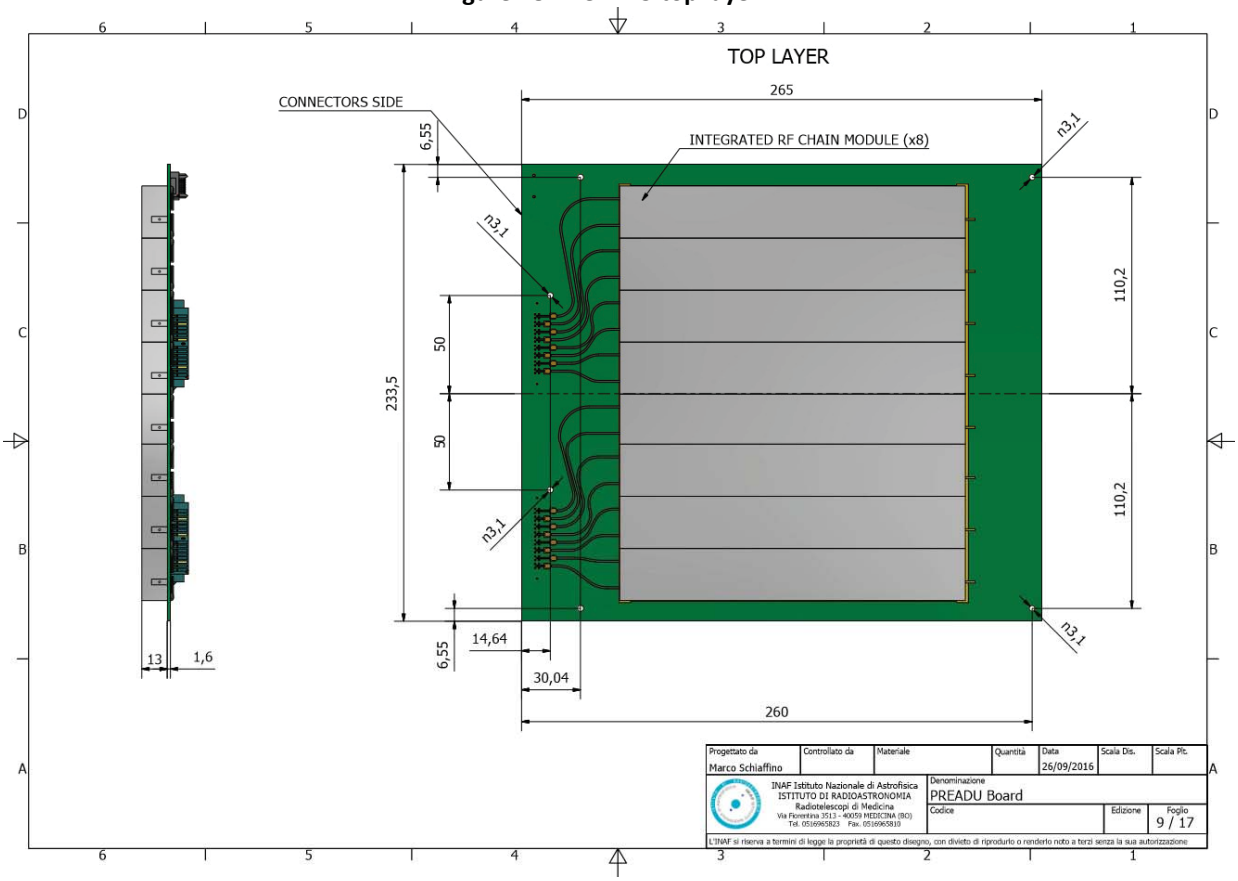
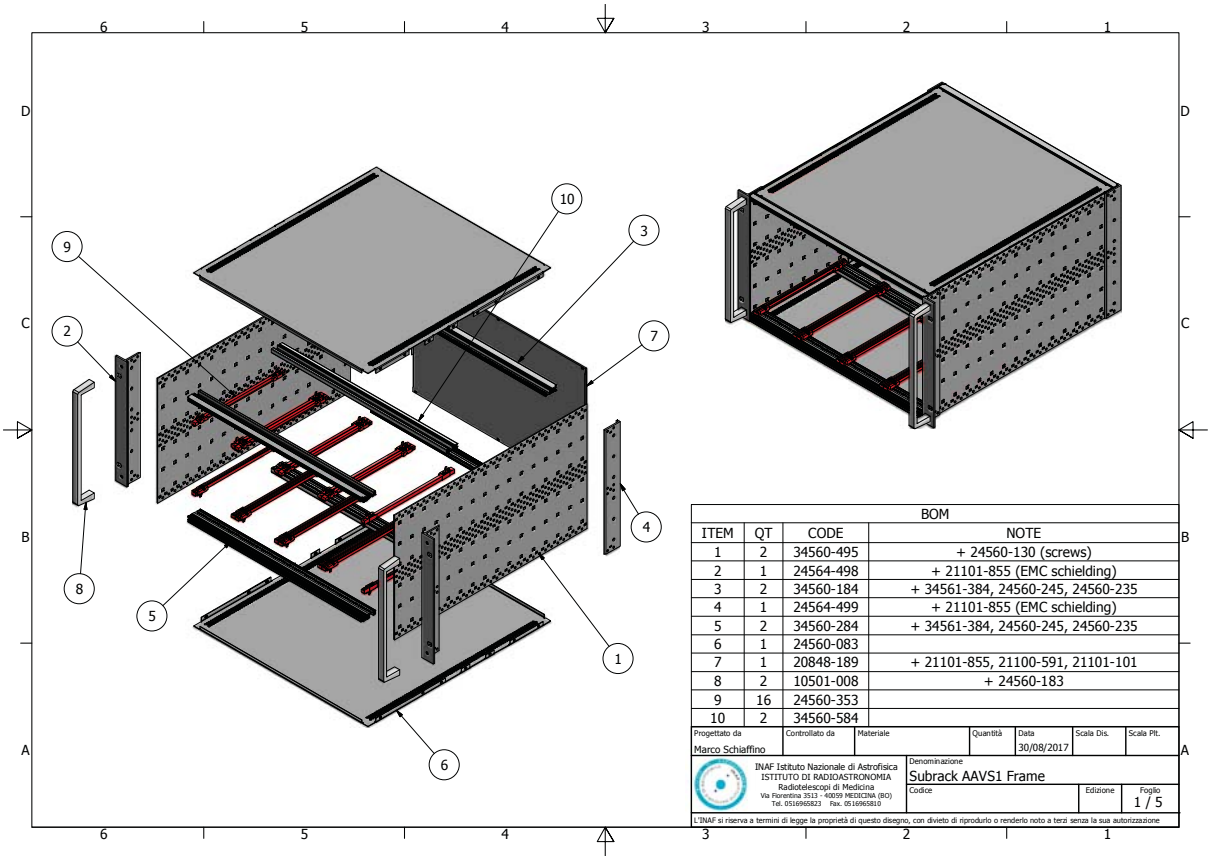


Figure 29. Pre-ADU (right) and a section with part volumes (left).



BOM			
ITEM	QT	CODE	NOTE
1	2	34560-495	+ 24560-130 (screws)
2	1	24564-498	+ 21101-855 (EMC schielding)
3	2	34560-184	+ 34561-384, 24560-245, 24560-235
4	1	24564-499	+ 21101-855 (EMC schielding)
5	2	34560-284	+ 34561-384, 24560-245, 24560-235
6	1	24560-083	
7	1	20848-189	+ 21101-855, 21100-591, 21101-101
8	2	10501-008	+ 24560-183
9	16	24560-353	
10	2	34560-584	

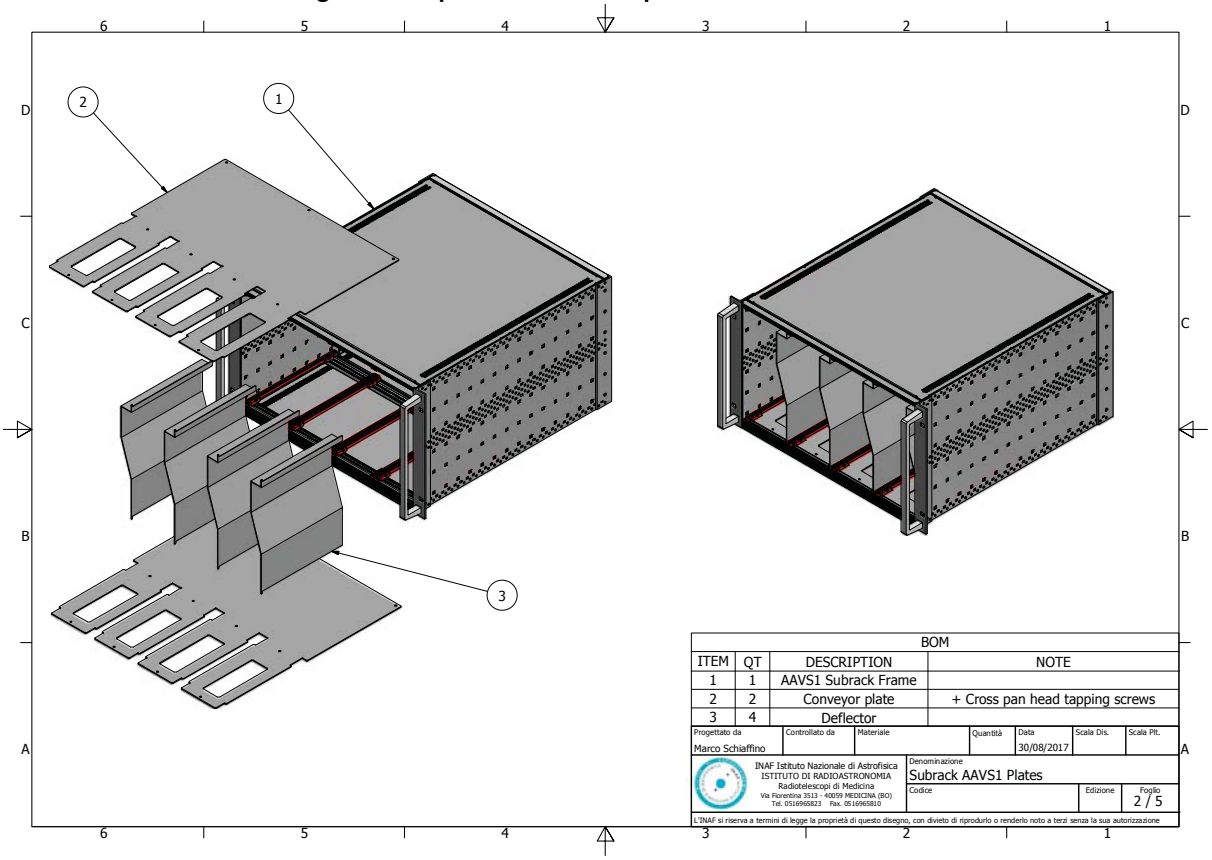
Progettato da: Marco Schiaffino | Controllato da | Materiale | Quantità | Data: 30/08/2017 | Scala Dis. | Scala Plt.

INAF Istituto Nazionale di Astrofisica
ISTITUTO DI RADIOASTRONOMIA
Radiotelescopi di Medicina
Via Fiorentina 3513 - 40059 MEDICINA (BO)
Tel. 0516965823 Fax. 0516965810

Denominazione: Subrack AAVS1 Frame
Codice | Edizione | Foglio: 1 / 5

L'INAF si riserva a termini di legge la proprietà di questo disegno, con divieto di riprodurlo o renderlo noto a terzi senza la sua autorizzazione

Figure 30. Expanded view with parts of a TPM sub-rack.



BOM			
ITEM	QT	DESCRIPTION	NOTE
1	1	AAVS1 Subrack Frame	
2	2	Conveyor plate	+ Cross pan head tapping screws
3	4	Deflector	

Progettato da: Marco Schiaffino | Controllato da | Materiale | Quantità | Data: 30/08/2017 | Scala Dis. | Scala Plt.

INAF Istituto Nazionale di Astrofisica
ISTITUTO DI RADIOASTRONOMIA
Radiotelescopi di Medicina
Via Fiorentina 3513 - 40059 MEDICINA (BO)
Tel. 0516965823 Fax. 0516965810

Denominazione: Subrack AAVS1 Plates
Codice | Edizione | Foglio: 2 / 5

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Figure 31. TPM sub-rack with air deflector.

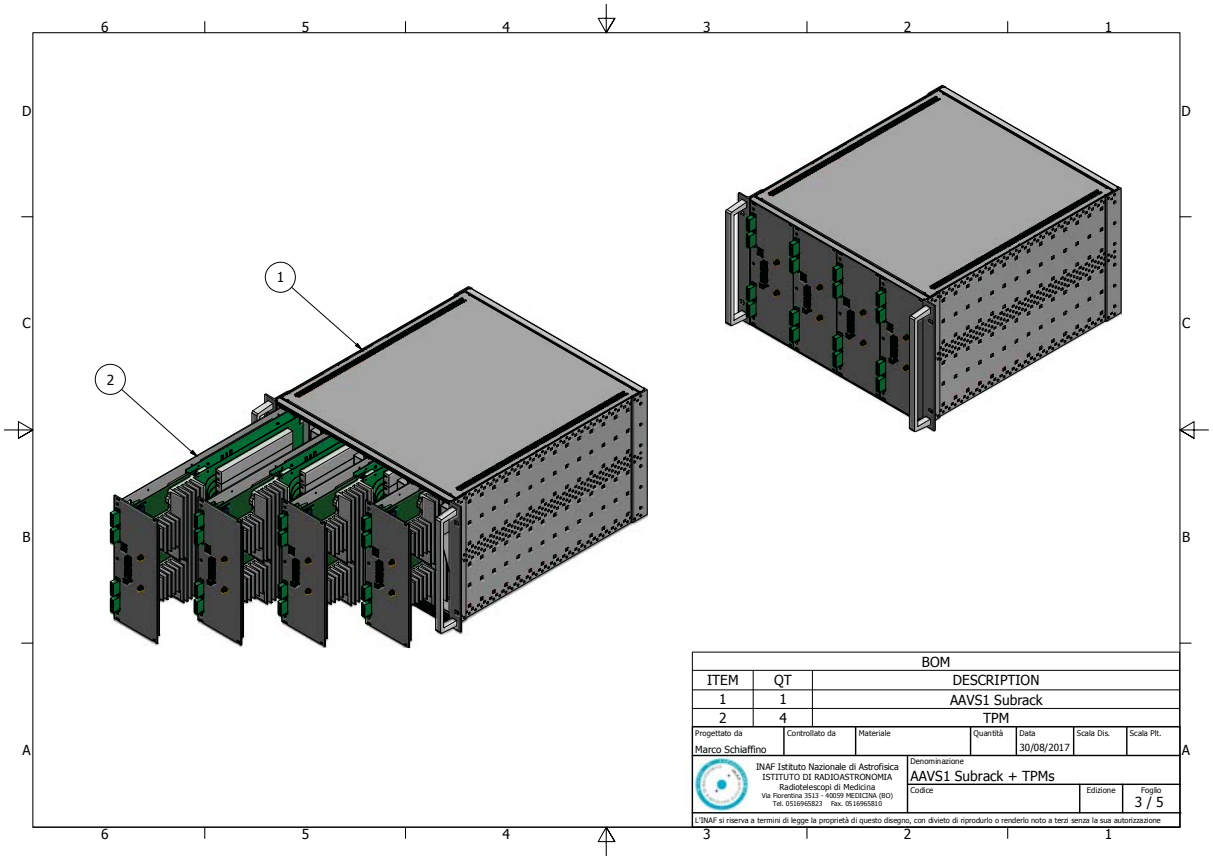


Figure 32. View of a complete TPM sub-rack with four TPM units (foreground). In the background, the four front panels are visible.

4.2.3 Firmware

A test firmware has been initially developed to support the verification of the FPGA interfaces, RF signal quality assessment and production tests. This firmware version implements all the FPGA interfaces, including DDR3, Ethernet and JESD204B, together with custom modules to generate and check data using the related interface. The same firmware supports ADC data acquisition storing the data in the FPGA internal memory (up to 2 Mbyte per FPGA) and transmitting the data snapshots over 1G Ethernet. The number of inputs to be stored in the internal buffer and their locations can be selected by software allowing the user to acquire data from adjacent inputs simultaneously.

The AAVS1 firmware followed two different development directions. DSP related firmware modules have been designed by INAF, while interfaces design and integration have been developed in Oxford. Enforcing a strict separation between DSP firmware and board support firmware and using standard interfaces for inter-modules communications permitted to work simultaneously on both parts of the design and facilitated the integration effort.

In the AAVS1 firmware the code previously developed for the test firmware has been largely re-used, this includes code implementing the FPGA interfaces, which was already verified and tested. DSP firmware modules followed an independent development flow and were verified separately before integration.

The FPGA Firmware is mainly coded in VHDL and structured in such a way to simplify the transition to different boards, FPGA vendors and families. Technology dependent code has been isolated into specific portions and industry-standard interfaces implemented to enable the communication

between main parts of the design; leveraging standard interfaces allows the designer to transparently modify the implementation of part of the design while maintaining compatibility with the rest of it.

The FPGA Firmware consists of a top-level board wrapper, which is customized to support the specific board pinout; the firmware is then partitioned into two main sections. An I/O ring section includes all external interfaces and technology dependent modules such as PLLs, transceivers and physical layers. The I/O ring is directly connected to the DSP section using industry standard busses. The following block diagram shows the separation between the two sections.

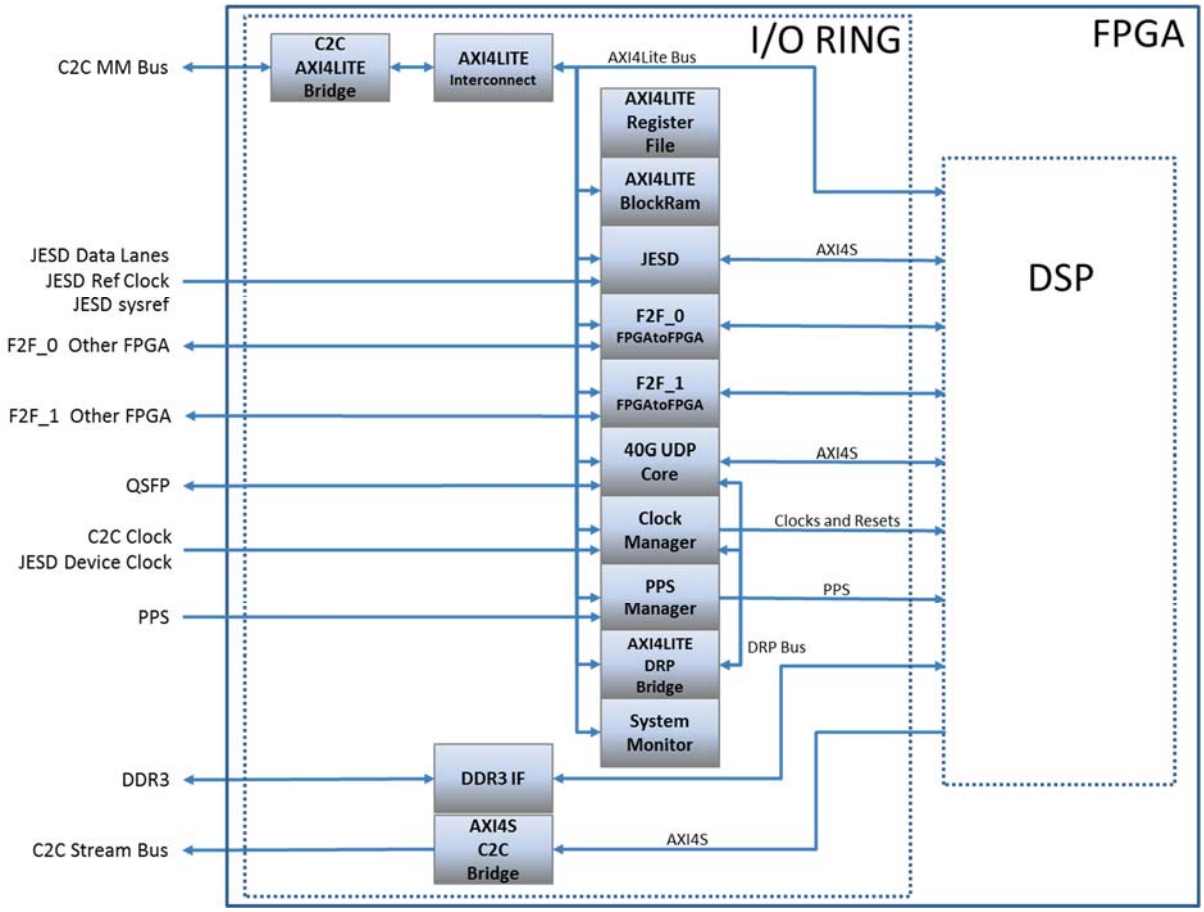


Figure 33. FPGA Top Level Firmware Block Diagram.

Figure 34. DSP section block diagram shows the DSP section block diagram which consists of several processing and monitoring modules. Both the internal communication between the implemented modules and external communications to the IO ring section make use of AXI4Lite interfaces to access the configuration registers implemented in each module and AXI4S interface to implement data streaming interfaces. Auxiliary modules monitor and extract data at several points along the processing chain; extracted data are forwarded to the IO Ring and transmitted on either 1G or 40G Ethernet. Some of the modules are encapsulated in a wrapper that manages the interface with the standard AXI4 stream interconnections and permits to select among different implementation architectures, when multiple architectures have been developed.

Further detail about FPGA firmware can be found in [RD15].

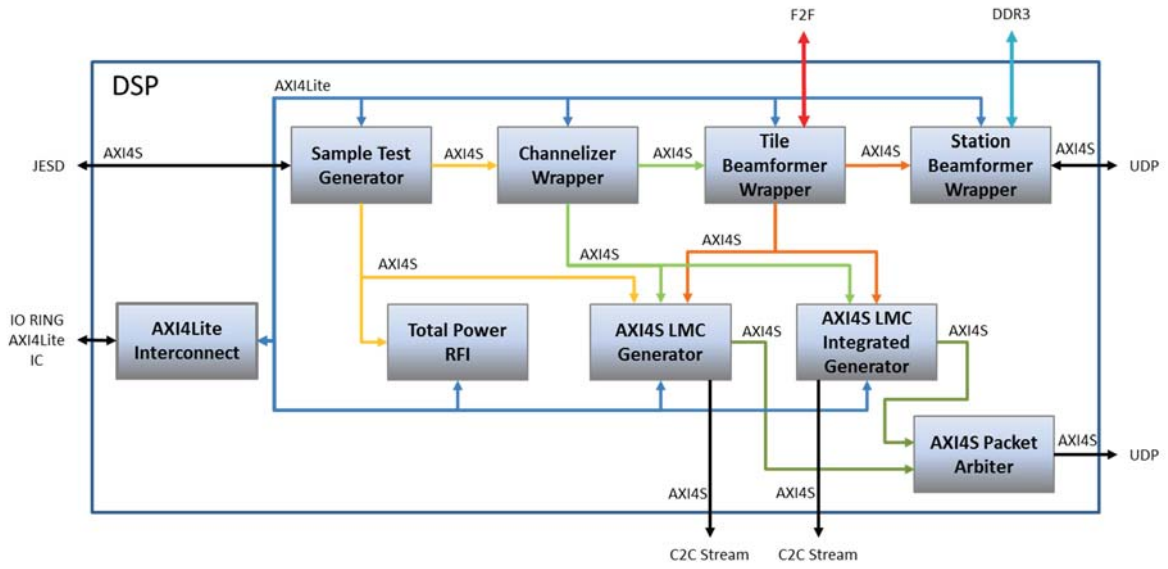


Figure 34. DSP section block diagram

4.2.4 Software

The operations required for monitoring, control and management of AAVS1 are a subset of those required for LFAA. The prototype and test implementations developed and deployed on AAVS1 are described in detail in [RD17] , with a summary provided below:

Hardware Monitoring and Control

AAVS1 is composed of several types of hardware, TPMs, network switches, PDUs, compute nodes, and so on. In the case of digital processing boards, firmware registers need to be accessed and updated to control a running observation. A software library, PyFabil, was developed to interact with TPMs. Interfacing libraries were also developed for the other hardware devices, including the 40Gb switch, PDU and compute server. These libraries are then wrapped as TANGO devices and controlled by the TANGO LMC system.

Data Acquisition and Correlation

The TPM can send control data which can be used for correlation, bandpass flattening and general diagnosis. The control software must be capable of acquiring and processing this data. Additionally, the control software should be capable of acquiring short segments of the partial and station beams for diagnosis. A high-performance data acquisition library wrapped with a Python interface was developed for this purpose. This library also includes the correlator which is required for calibrating the stations.

Calibration and Bandpass Flattening

The LFAA needs to send calibrated, flattened station beams to CSP. Bandpass flattening occurs on the TPM, however truncation parameters (one per group of 8 channels) must be calculated in software. Calibration is required to compensate for environment and instrument induced noise (gain and phase offsets). The L1 requirements for LFAA state that the calibration cycle must be performed every 10 minutes, such that every usable frequency channel must be calibrated every ~1.5 seconds. To this end, a pipelining library was developed which is used to implement the calibration, bandpass flattening and pointing functionality. This library is introduced in Section 7 of [RD15], where the bandpass flattening and calibration pipelines are also described.

Pointing
To point a station beam toward a sky location, phase coefficients must be applied to each antenna and frequency channel. A delay and delay rate per antenna need to be computed by the pointing software, whilst the delay per channel are then calculated on the TPM. The delays and delay rates need to be updated periodically to observe fixed source on the sky.

System Configuration and Management
The AAVS1 deployment at the MRO consists of four cabinet housing TPMs, network switches, PDUs and the LMC server, amongst other equipment which cannot be controlled. The deployment is all managed through software deployed on the LMC server, which also controls the network configuration. Additionally, the LMC server itself has multiple server modules deployed, some of which run in virtualised environments.

TANGO LMC and AAV1 Backend
The TANGO LMC system is the control system prototype for AAVS1. It combines the software packages described above into a single system with a single controlling entity. The AAVS1 backend provides a flattened interface to the telescope, such that external users need not be aware of how the internal components are set up, or what technologies are being used. It also makes it easier to change internal components, if required, without affecting the communication mechanism with external entities.

Telescope Manager Emulator
The LFAA software system is regarded as a non-intelligent system managed by TM. TM is responsible for, amongst other operations, scheduling observation, decide what happens when faults arise and archiving LMC data. To prototype the interaction between LFAA and TM a TM emulator was developed for AAVS1. It implements a small subset of TM's functionality, essentially those are required for the proof-of-concept of configurability of the LFAA software system.

4.2.5 Signal model

Different models have been written to simulate the performance of the system.

- The antenna system has been simulated using finite element electromagnetic simulation. This provides information about antenna pattern, cross talk and mutual coupling between antennas.
- The receiver section has been simulated using a RF simulator (Genesys), in the frequency domain [RD2]. This provides information about gain, spectral response, and intermodulation products due to nonlinear behaviour.
- The digital section, including quantization effects, have been simulated using an end-to-end MATLAB model, in the time domain.

Each model provides a performance analysis of the modelled section. A more complete analysis is possible by combining the models. As they operate on different performance parameters, and in different domains, this is not straightforward. The adopted strategy consists in:

- The antenna model is used to derive a typical frequency response for this element. Typical scatter from the average response is also derived.
- The receiver model also provides a typical frequency response, and response distribution. In addition, given a list of observed RFI frequencies and levels [RD39], a list of intermodulation products is generated. It is assumed that the RFI aggressors are monochromatic lines.
- The information is used to generate a time domain signal for the digital section simulator. The signal is composed of a Gaussian noise, with a spectrum obtained from the sky spectrum

modified by the antenna and receiver bandpass, a set of RFI signals (same of the previous step, this time considered as broadband pseudorandom noise, smoothed to about 1 Hz bandwidth), and a set of monochromatic lines corresponding to the intermodulation products.

The MATLAB model produces a simulated beamformed signal, which is processed by a simulated and idealized version of the CSP and SDP. Passband effects are removed in an idealized calibration (instrumental effects are known a priori) and the final resolution is that of the zoom mode CSP channelizer.

4.2.5.1 *Receiver analogue model*

For the design of the receiver and to be "compliance" with the project requirements, an analysis was carried out beforehand in which the specifications to be complied with were obtained.
Starting from these numbers, deduced analytically, a drawing was created with real RF blocks (amplifiers, filters, attenuators). To verify if the RF implementation chosen was able to meet the specifications obtained previously, various simulations were then carried out to evaluate the system performance (NF, G, IP2 / 3, P1dB).

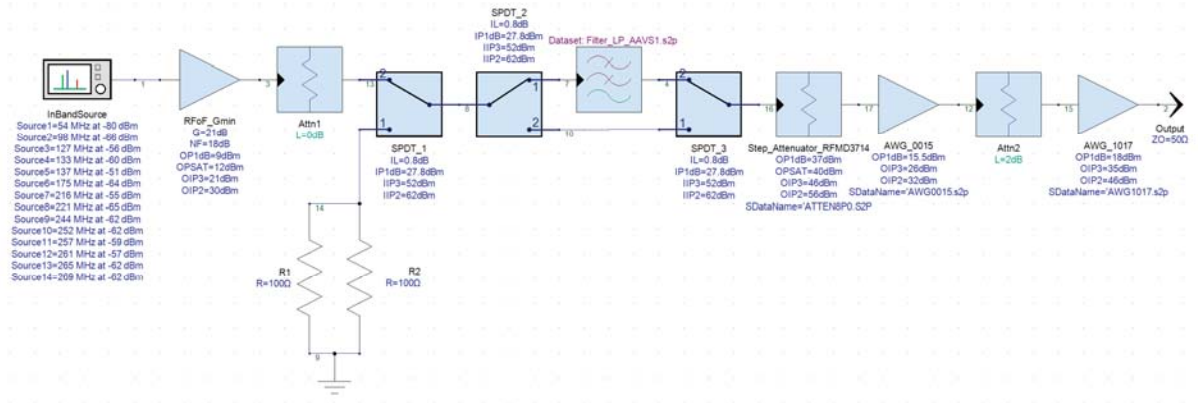


Figure 35. AAVS1 RX chain design for Spectrasys simulation

For the specific case of the evaluation of the non-linearities at the output of the receiving chain, since the RFI scenario received by the antennas is very complicated and composed of very different signals both in non-constant spectral distribution and in amplitude, a simulation has been performed with a specific tool called Spectrasys (included in Keysight's Genesys package).
Genesys Spectrasys is a powerful RF system simulator that enables a system architect to quickly arrive at the optimal architecture to avoid system integration issues downstream. Unlike spreadsheet calculations, Spectrasys offers accurate system model libraries that accounts for nonlinear harmonic generation, impedance mismatch as well as forward and reverse propagation of fundamental, harmonic and mixing signals. Its unique interactive root cause analysis identifies the origin of any undesired spurious signals so that corrections to the architecture can be made during the design stage and not during system hardware integration.
We used as a test signal a series of spectral lines corresponding to the strongest RFI aggressors measured at the site. The model then evaluates the presence of intermodulation terms at the output, taking into account element nonlinearities, responses and mismatches. The RFI data were obtained by Sutinjo *et*. *al*. at the MRO site (WA) in 2013 [RD39]. Figure 36 shows the measurements made with a passive antenna (SKALA-2) with a 3:1 balun. This data has been subsequently corrected to incorporate the mismatch loss of the balun with the antenna, which shows up to a 30dB increase in the low frequency (out of band) RFI between 10 to 30 MHz. A further reduction of the low frequency

RFI is due to the LNA passband and input mismatch. This has been used to evaluate the tone frequencies shown in Figure 35.

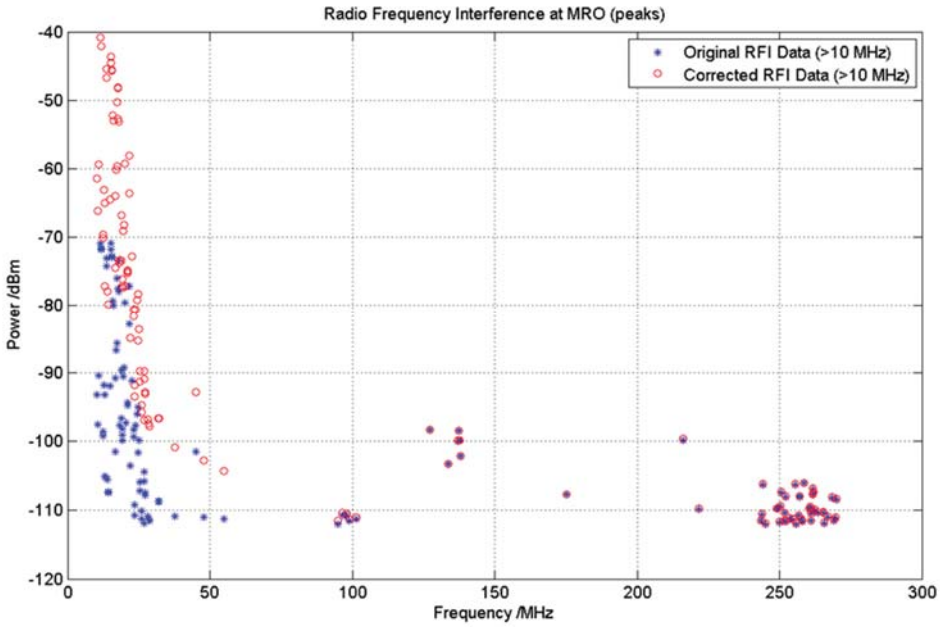


Figure 36. RFI measured at the MRO site. Data subsequently corrected for the balun mismatch loss to show expected RFI levels at the antenna.

Spectrasys analysis provides a list of tones, included the amplified version of the RFIs, at the ADC input. Stronger aggressors are amplified about 88 dB above what shown in Figure 35. Intermodulation products are shown in blue, and are about 55-60 dB below the aggressors, extending up to 800 MHz.

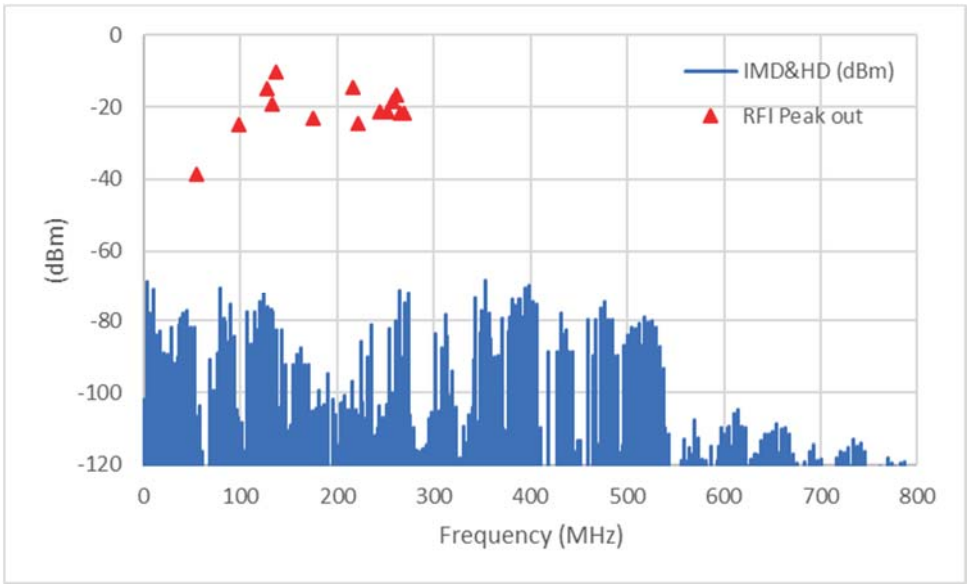


Figure 37. Output of Spectrasys simulation (intermodulation and harmonic distortions in blue)

These lines have been used in the subsequent analysis, using the Matlab simulator.

4.2.5.2 *MATLAB signal model*

A simplified block diagram of the functional model for the signal processing chain is described in Figure 38. The signal processing model is written in MATLAB and operates in the time domain. It is composed

of a signal generator, which produces a time domain signal as close as possible to the actual digitized signal, the actual signal processing model, which produces one or more data streams, an analysis module, which computes a fine channelization of the beams, auto and cross correlation. Result is integrated for a prescribed total integration time and the resulting calibrated visibilities stored in a disk file.

Due to memory and computing power limitations, only a limited number of antennas can be simulated. The model either products visibilities for two individual antennas, or generates a single beamformed sample stream, for which only autocorrelation is computed.

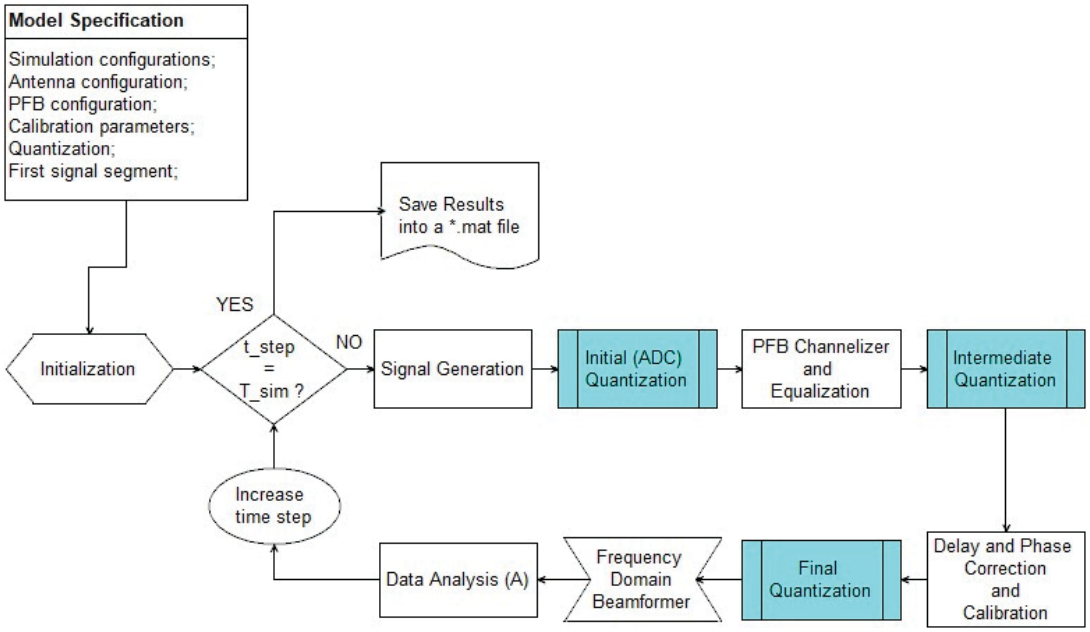


Figure 38. Signal processing model flow diagram.

The signal generator produces partially correlated Gaussian noise, with an arbitrary spectrum both for correlated and uncorrelated part. The uncorrelated part is independently generated for each antenna, while the correlated part is generated once and delayed for the time varying geometric delay in each antenna. An arbitrary number of sinusoidal tones are added to this noise, to simulate monochromatic RFI sources, or intermodulation products. Due to limited information on the RFI spectral content, RFI is simulated as an added random noise, with a spectrum obtained by smoothing the RFI measurements using a 1 MHz window.

An example of the signal spectrum at the ADC input is shown in Figure 39. Result is close to actual measurements in Table 7.

The model simulates all signal processing steps, from initial conversion to digital to beamforming. The model uses real numbers forced to integer values, for computational speed, and closely reproduces all the major requantisation steps and the algorithms used in the FPGA. The result is very close to be bit accurate, with minor differences due to computational shortcuts.

The analysis portion simulates the data processing in the CSP, with a simplified but realistic model of the zoom mode imaging correlator and of the final calibration procedure. All instrumental effects due to signal processing (rescaling, digital equalisation, channeliser bandpass) are removed, together with the antenna and receiver gain assumed in signal generation.

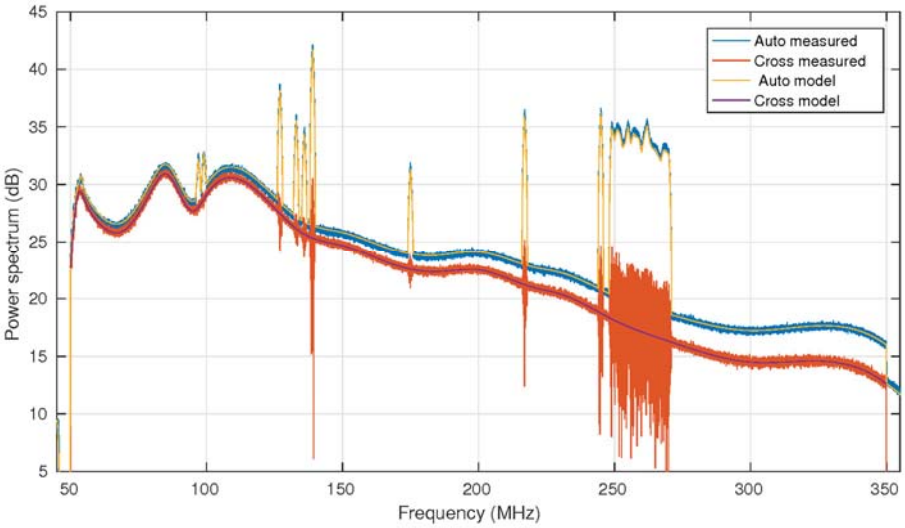


Figure 39. Autocorrelation and cross-correlation spectra for two simulated antennas

Scope of this model is:

- Validate the signal processing algorithm. Although the VHDL code is tested using regression tests, these are very computer intensive and can be performed only for short time sequences.
- Evaluate effects of the quantisation, especially for the ADC, with a realistic input signal
- Evaluate effects due to RFI (saturation, intermodulations).

Input signal depends on results from other simulators. The input spectrum depends on the antenna and LNA passbands, and form attenuation of the passband filter in the signal conditioning module. RFI analysis depends on RFI measurements, and intermodulation products computed in the receiver analogue model.

An example of quantisation analysis is shown in Figure 40. Quantisation noise is shown from different

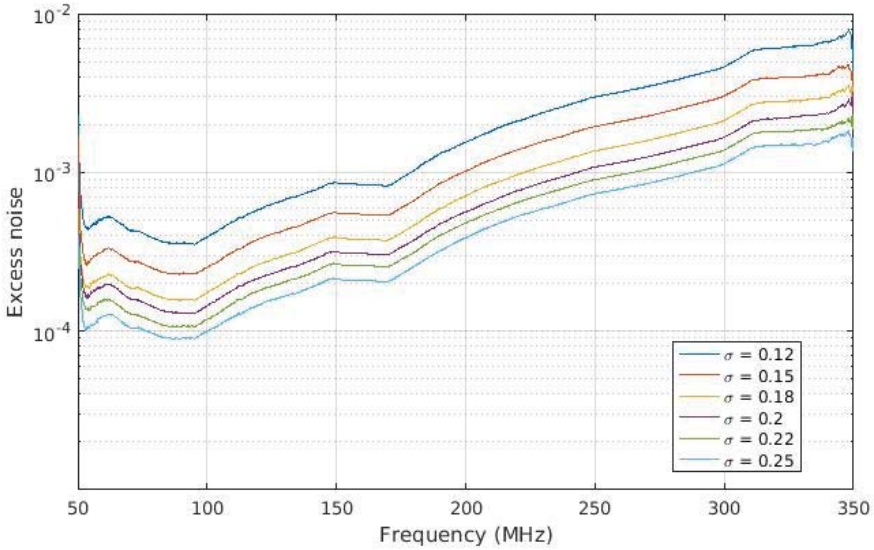


Figure 40. ADC quantisation noise vs- frequency and input level

RMS input levels ranging from 12% to 25% of the ADC clipping level.

To model the effect of RFI intermodulation products, derived by the Spectrasys model, we selected the strongest intermodulation tones and added them to the noise. To reduce the computational time, increased also due to the large number of simulated tones, the number of antennas in the station has

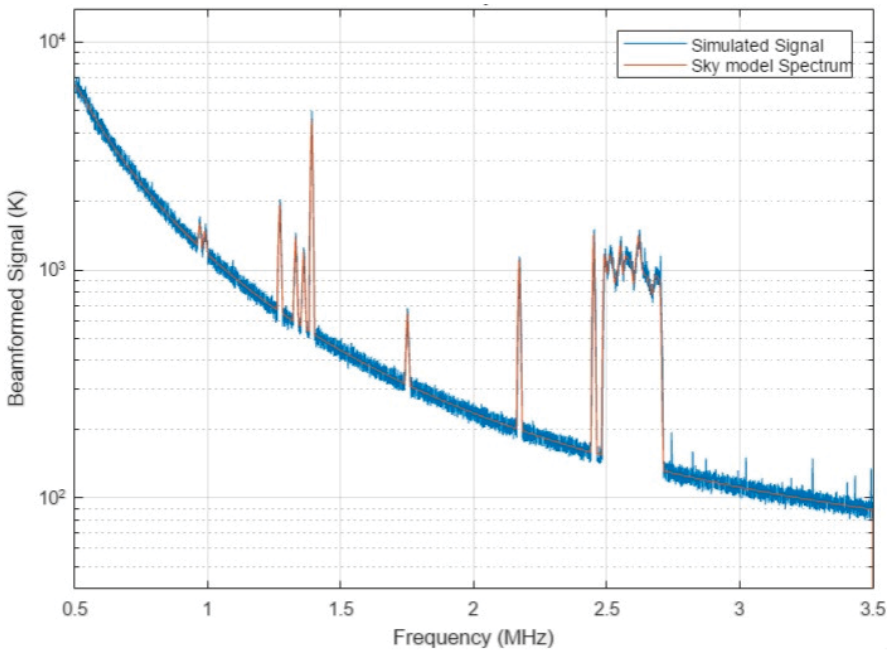


Figure 41. Simulated station spectrum - 32 antennas with RFI

been limited to 32 and the integration time to 100 ms. To increase the effect of the intermodulation products to an equivalent integration time of 1000 s, their amplitude has been increased by 20 dB. After calibration, correction for filter bandpass and other known signal processing artefacts, the result is shown in Figure 41, using a resolution bandwidth of 7.2 kHz, close to the imaging mode correlator resolution. The expected beamformed spectrum is also shown in red. Correspondence of the model result is very good, in particular the LFAA channeliser bandpass ripple is accurately cancelled. Some spurious tones are visible (at 1000 seconds equivalent integration time) near the high end of the spectrum, where the sky signal is lower.

The fractional noise (i.e. the ratio of the actual to the expected signal, normalized to its RMS value) is shown in Figure 42. Regions heavily affected by RFI have been deleted. Intermodulation tones are

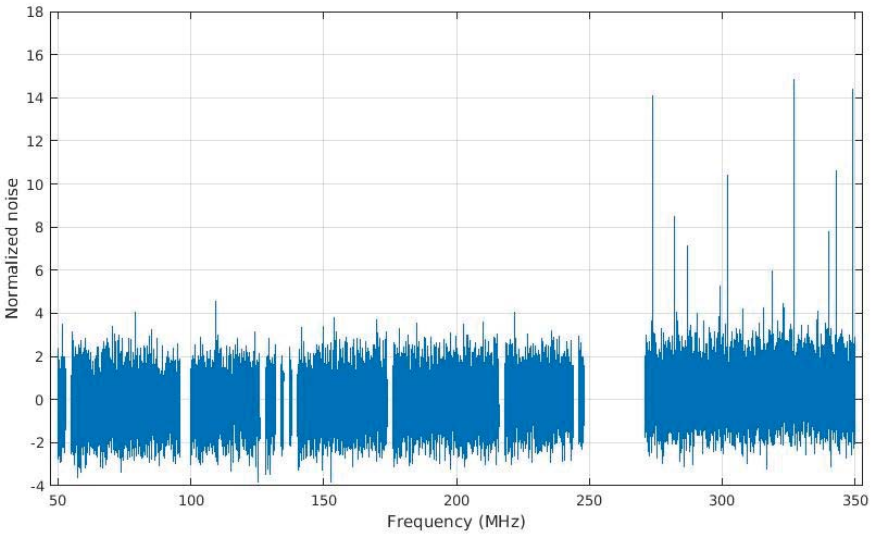


Figure 42. Effects of intermodulation tones for 1000 s integration time

more clearly visible, but only in the high part of the spectrum.
For a more accurate simulation a better characterisation of the RFIs must be performed, including their spectral content.

4.3 Verification of Progress

Two types of test have been defined for ADU boards: performance test and production test. The former characterizes the behaviour of the boards in the RF environment, while the latter provides the functional verification of the boards.

The progress of the SPS prototyping activities has been tracked with the following mechanisms:

1. Testing in lab (functional/performances and acceptance tests)
2. On field testing.

5 Test Results

5.1 RX tests

The verification of RX (Front End and pre-ADU), followed a specific test plan that has evolved from the single prototype measurement to the AAVS1 production verification.
We would remind that a complete RX chain it is necessary because it is not possible to break the system in two part and characterize them separately due to the optical fibre in the middle.

Mainly test procedures are based on the same principles. They consist of three main steps with the aim of achieving the complete characterization described below.

5.1.1 Production test

The company that produces the boards/modules performs this preliminary test; it is fast and simple and consist in a visual check of the correspondence between the production and the mechanical drawings.

5.1.2 Functional test

This test involves the verification of the boards/modules in two ways:

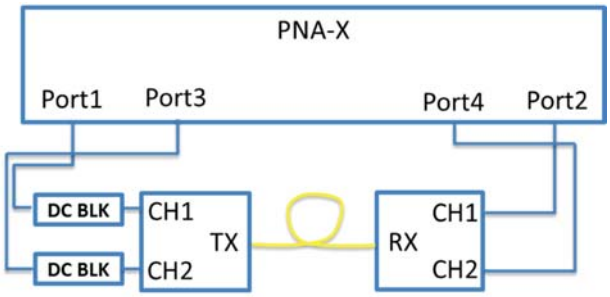
1. Electrical test: current consumption measurement with a 3.5V of power voltage;
2. RF test: gain and input/output return loss for at least 50, 350 and 650MHz.

5.1.3 Qualification- Performances test

This is the deepest test which lead to a fully characterization of the modules. Not all tests will be performed for each module delivered but only the basic ones (Sxx, Non linearities, NF)

5.1.3.1 *S-parameters and Isolation*

S-parameters measurement shall be performed with an Agilent 5249A PNA-X 4 port VNA. This way is evaluated even the isolation between the two optical wavelengths (i.e. RF channels); complete reports with accurate tests are reported in [RD5], [RD30], [RD38].

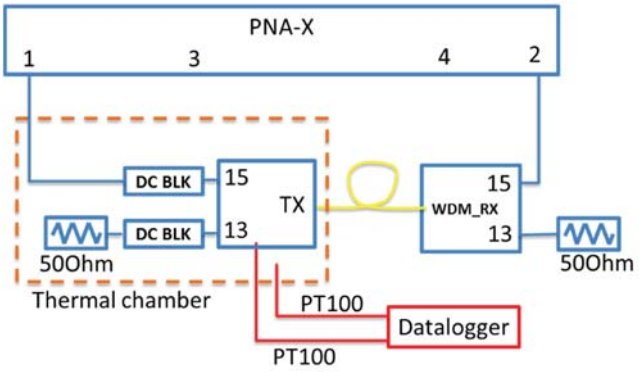


Parameter	Value
Start frequency	10 MHz
Stop frequency	1 GHz
Number of points	1601
Power	-30 dBm
IF bandwidth	300 Hz
Calibration	Full 4 Ports
Calibration kit	ECAL-N4431-60008

Figure 43. PNA-X VNA setting for S-parameters and Isolation measurements.

5.1.2.3 *P1dB compression point*

The input P1dB compression points shall be measured using PNA-X Agilent 5249A in CW power sweep mode (from -30 to 0dBm) at different temperature.

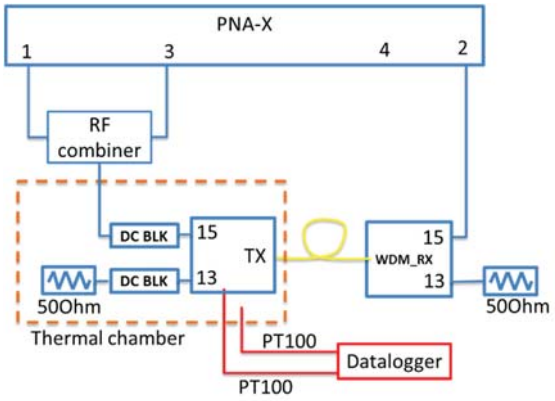


Parameter	Value
CW frequencies	50-650 MHz with 50MHz step
Number of points	1601
Power sweep	-30 to 0 dBm
IF bandwidth	300 Hz
Calibration	Full 4 Ports
Calibration kit	ECAL-N4431-60008

Figure 44. P1dB compression point measurement set up and PNA-X configuration.

5.1.2.4 *Non linearities*

The second and third intermodulation products (IP2/IP3) shall be determined using two tones distortion measurement. In the measurement setup the PNA-X 5249A will be used to supply the two tones with 1MHz spacing, at a specific power level and frequency, into the RFoF link. The tones will be combined using a Minicircuits ZFSC-2-2 power splitter and provided at one input of the RFoF link. Input power level at the fundamental frequency will be set at 0dBm at the RFoF link output.
The power level of the fundamental tones and intermodulation products will be measured using the PNA-X, which calculates OIP3 and OIP2 simultaneously vs frequency. These measurements can be made even at different temperatures using the thermal chamber.

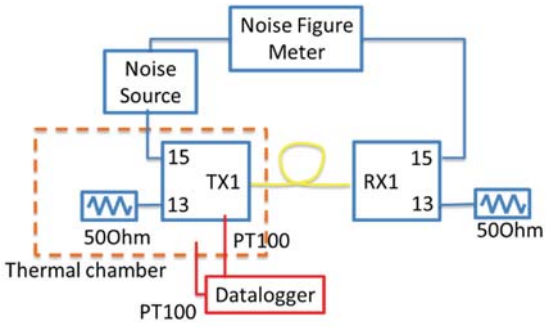


Parameter	Value
IF bandwidth	300 Hz
Marker	Peak
Points	201
Ref Level	+10 dBm
Calibration	Source & Receiver Power

Figure 45. IP2/IP3 measurement setup and VNA configuration.

5.1.2.4 *Noise Figure*

Noise Figure shall be measured using the HP8970B Noise Figure Meter with an Agilent 346A Noise Source at different temperature.

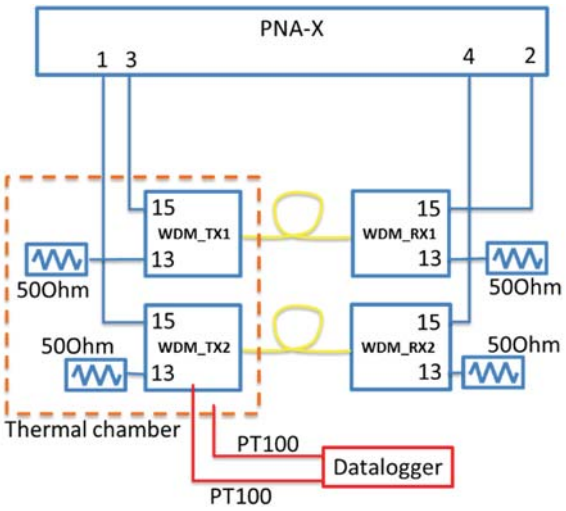


Parameter	Value
Smoothing Factor	16
F start	10 MHz
F stop	1000 MHz
F step	10 MHz
Calibration	Noise Figure & Gain

Figure 46. NF measurement set up and HP8970B configuration.

5.1.2.5 *Gain module and phase stability*

Gain module and phase stability test shall be measured using PNA-X 5249A. A couple of Transmitters should be placed inside a thermal chamber where the temperature variation and slope can be set up and logged through a datalogger.

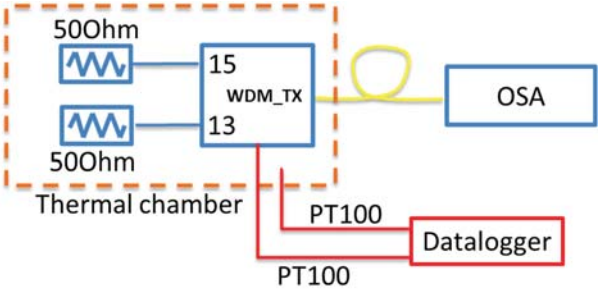


Parameter	Value
IF bandwidth	1 kHz
Ref Level	+10 dBm
Marker	Peak
Points	7
F start	50MHz
F stop	650MHz
F step	100MHz
Average n.	16
Average type	Sweep by sweep
Calibration type	Response
Calibration kit	ECAL-N4431-60008

Figure 47. Gain module and phase stability measurement setup and VNA configuration.

5.1.2.6 *Delta Lambda vs Delta Temperature*

Peak emission wavelength shall be measured using an Optical Spectrum Analyser (OSA) MS9740A. After the stabilization of the temperature inside the chamber and of the modules can be acquired the data with OSA.



Parameter	Value
RBW	1kHz
VBW	1kHz
Points	10001
λ_{start}	1300
λ_{stop}	1560
Resolution	0.07nm
Calibration	Alignment, Resolution and Wavelength
Marker type	Lambda

Figure 48. Delta Lambda vs Delta temperature measurement setup and OSA configuration.

5.1.4 Automatic test bench for RX system

As we mentioned before, this paragraph describes the procedure we followed to verify the specifications of the 440 AAVS1 receivers.
Considering using a single instrument for each single measurement in the laboratory, a complete characterization of the first 40 pre-production required 3 working days (about 1 hour per chain without report production) and aware about that, it has been necessary to reduce measurement time. For doing that a solution that automates the bench minimizing the variability of the measurements due to manual connections, the changing of internal attenuator and fastening the data storage, has been prepared.
The first mandatory step was to upgrade Keysight's PNA-X N5249A instrument, through Option 423, which allows to have an internal combiner and generate the dual source for intermodulation measurements and option 029 to make very accurate noise measurements with the Cold Source method. Thanks to these and Keysight 87222C transfer switches with Keysight 11713B driver switches, it was possible to characterize a complete receiving chain and produce its report in about 8 minutes. Below you can see the configuration of the test bench after the upgrades.

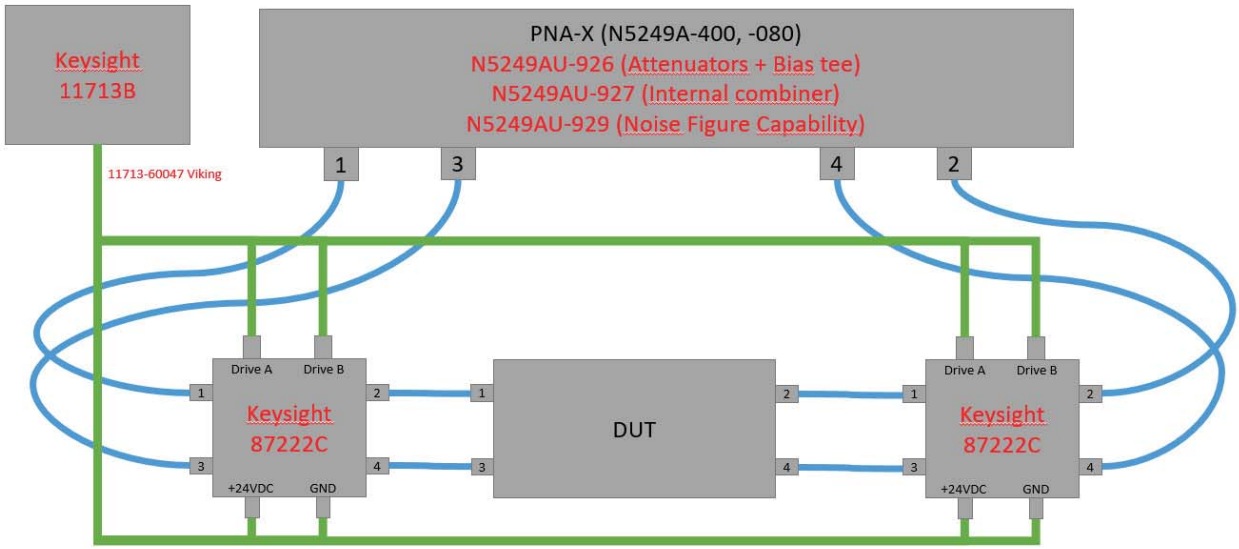


Figure 49. AAVS1 test bench connection scheme.

This measurement system must be able to qualify each of AAVS1 RX, in terms of power consumption (DC power) and Radio Frequency. Using Matlab2016b scripts, these measuring instruments are programmed, interconnected and synchronized. After measurements, it is automatically produced the report required by AADC consortium. Following is the block diagram of the test bench used for AAVS1 receivers. DC blocks (Minicircuits BLK-89) are needed to prevent DC output from the Front-End RF ports to the PNA-X ports.

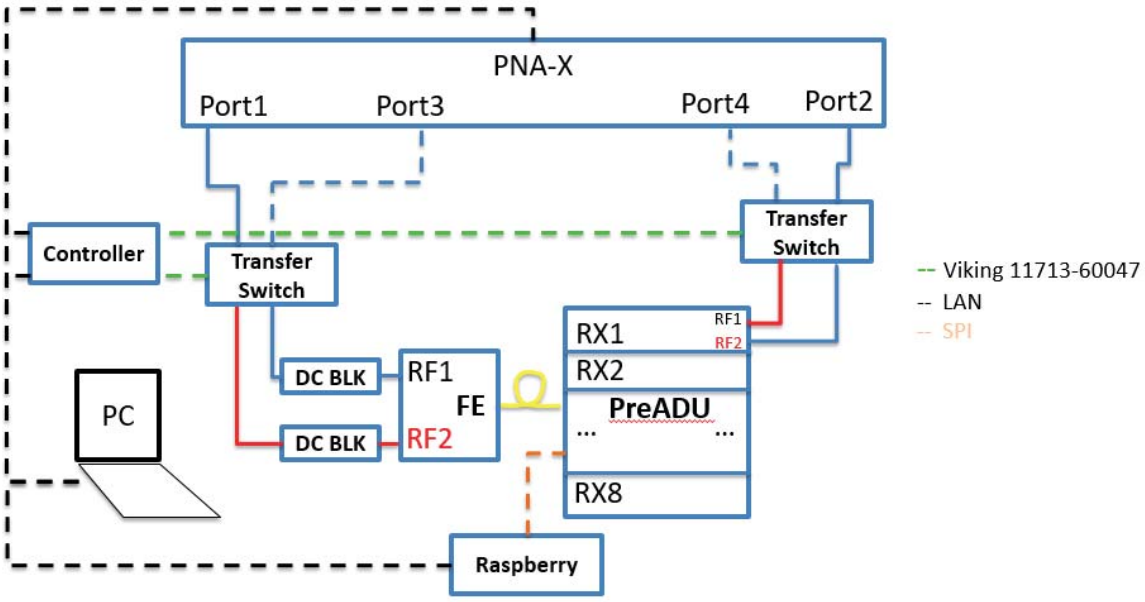


Figure 50 - AAVS1 test bench block scheme.

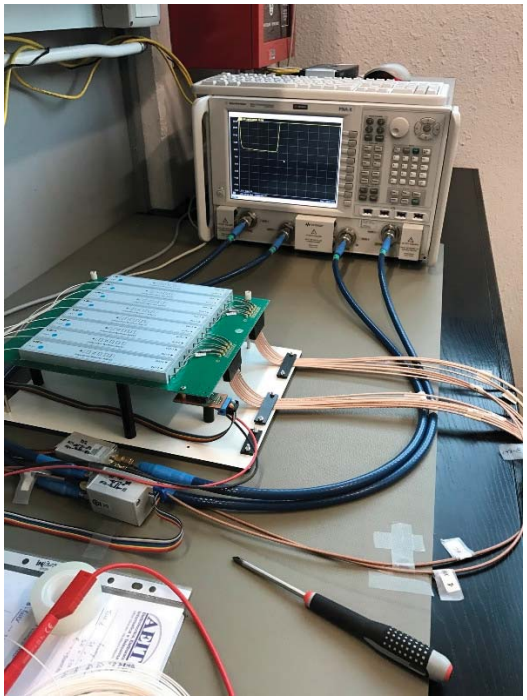


Figure 51. A picture of the developed test bench.

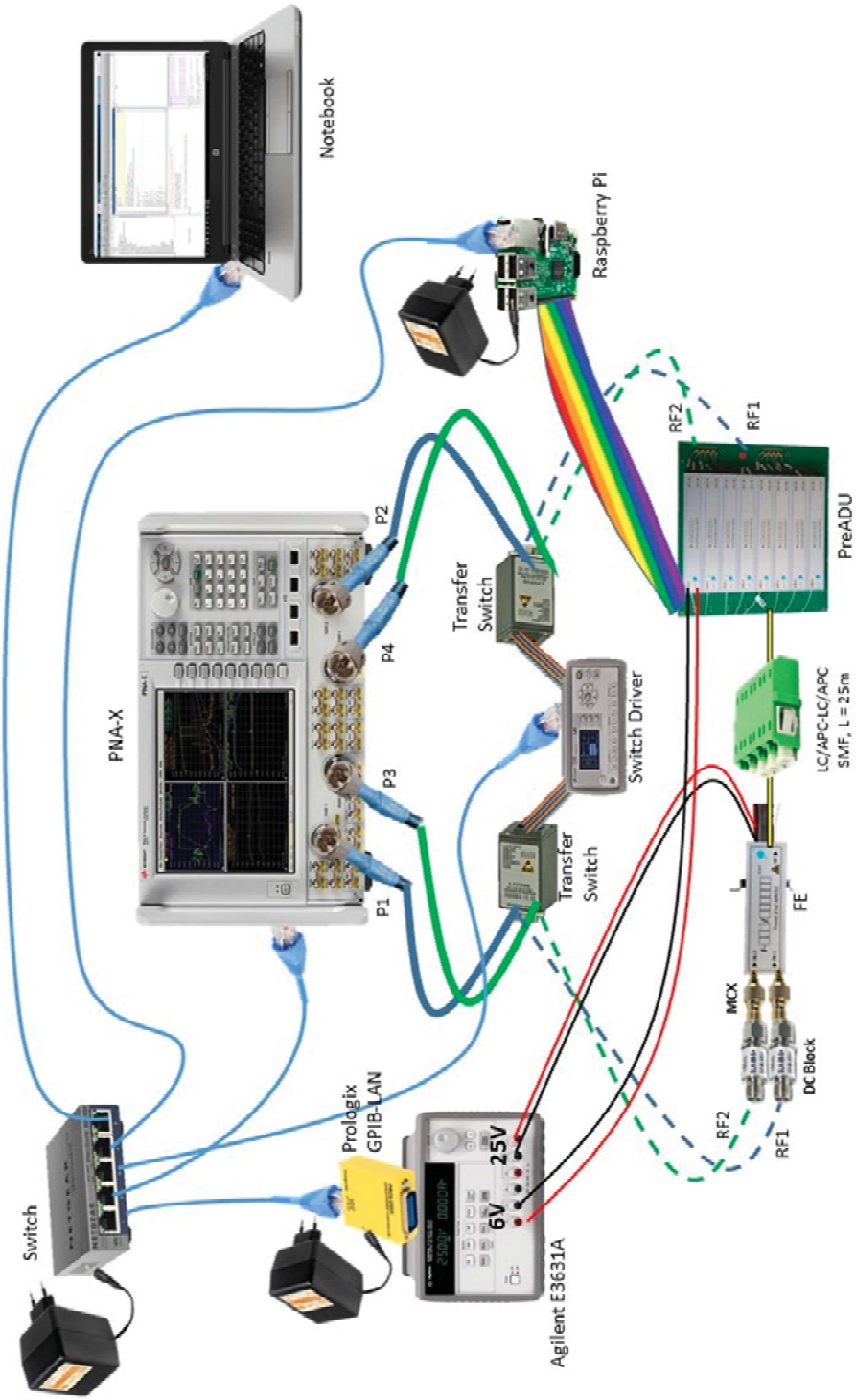


Figure 52. AAVS1 test bench scheme.

INAF	
Report date	05/09/16
Measure date	05/09/16
SN	F-001/201607

Parameter	Nominal Value	Note/Conditions	Measured Value	Test
Power FE consumption	<650mW	At room temperature with Vin=3.5V and without the LNA boards connected and biased.	0.586mW	Pass
Power ORX-RF consumption	<1250mW	At room temperature with Vin=3.5V. The value is obtained dividing by 8 the total absorption of a complete PREADU.	1.148mW	Pass
Flatness	+/-1.5dB	Measured in the two separate sub-bands: LB(50-375MHz) & HB(375-650MHz).	+/-1.4dB RF1 +/-1.3dB RF2@LB +/-1.1dB RF1 +/-1.0dB RF2@HB	Pass
High Pass filter rejection	>=45dB	Freq<=20MHz (+/-5MHz).	24MHz RF1 24MHz RF2	Pass
LB filter rejection	>=45dB	Freq>=450MHz (+/-5MHz).	430MHz RF1 431MHz RF2	Pass
HB filter rejection	>=45dB	Freq<=325MHz & Freq>=750MHz (+/-5MHz).	323MHz RF1 and 322MHz RF2@HP 725MHz RF1 and 726MHz RF2@LP	Pass
Gain	Min 54dB, Max 66dB	Freq=100MHz, FE connected directly to ORX-RF module with DSA at the minimum attenuation level.	60.0dB RF1 59.2dB RF2	Pass
IRL	>12dB	Measured at the FE input (50-650MHz band).	12.2dB RF1 13.4dB RF2	Pass
ORL	>12dB	Measured at the ORX-RF output. Measured separately in the two sub-bands LB and HB.	21.0dB RF1 and 21.1dB RF2@LB 21.6dB RF1 and 21.8dB RF2@HB	Pass
NF	<16dB	Measured separately in the two sub-bands, FE connected directly to the ORX-RF module with DSA at 16dB attenuation level.	10.7dB RF1 and 10.8dB RF2@LB 9.8dB RF1 and 9.9dB RF2@HB	Pass
RF channel isolation	>30dB	Defined as the difference between the measured gains at the two outputs of the ORX-RF module with the same input of the FE. Measured on both bands LB e HB with DSA at the minimum attenuation level.	58.0dB RF1 and 57.8dB RF2@LB 54.5dB RF1 and 51.3dB RF2@HB	Pass
OP1dB	>17dB	Freq=100MHz, FE connected directly to the ORX-RF module with DSA at the minimum attenuation level.	17.9dBm RF1 and 18.0dBm RF2	Pass
OIP3	>18dB	Freq=100MHz, FE connected directly to the ORX-RF module with DSA at the minimum attenuation level.	31.3dBm RF1 and 30.6dBm RF2	Pass
OIP2	>38dB	Freq=100MHz, FE connected directly to the ORX-RF module with DSA at the minimum attenuation level.	45.0dBm RF1 and 48.4dBm RF2	Pass

Figure 53. An extract of the test report.

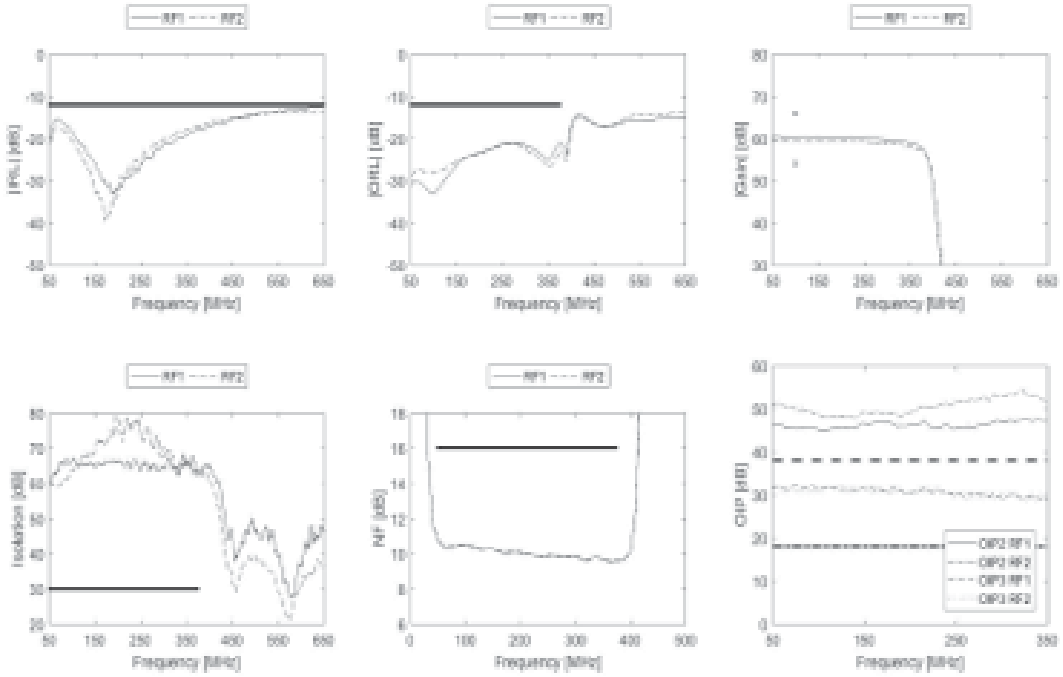


Figure 1 – Measurements with LB selected.

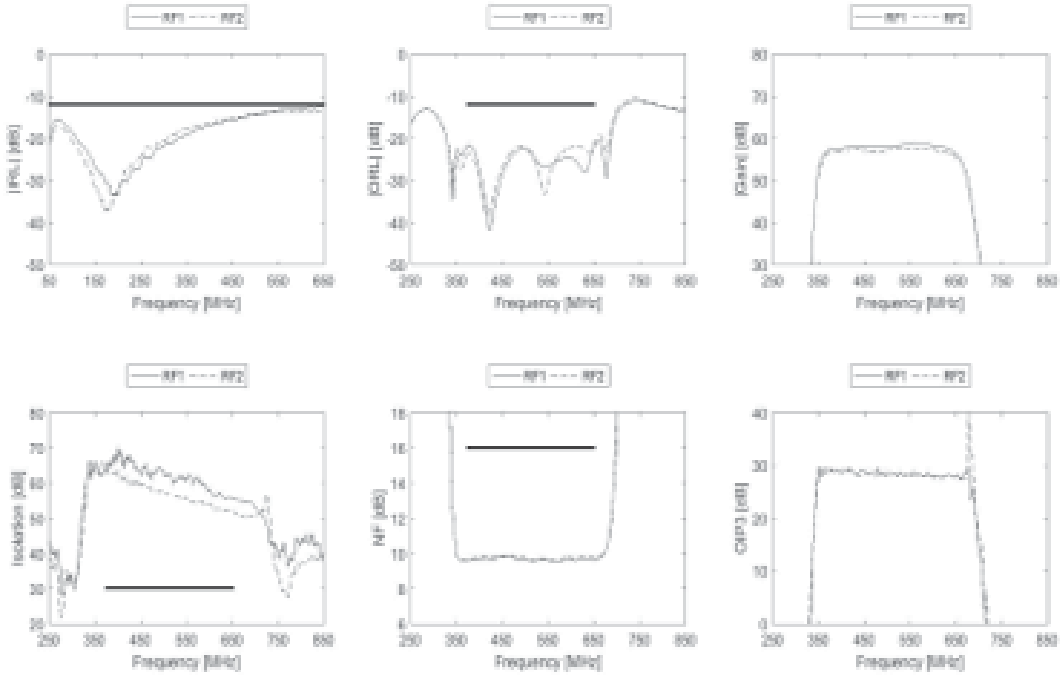


Figure 2 – Measurements with HB selected.

Figure 54. An extract of the test report.

5.1.5 EMC compliance tests

On November 2016 ICRAR performed for the Pre-ADU EMC tests.
The equipment has been tested against the applicable standard and was found to comply with the requirement (20dB below MIL-STD461F). It was suitable for deployment at the MRO as part of AAVS1 from an EMC point of view.

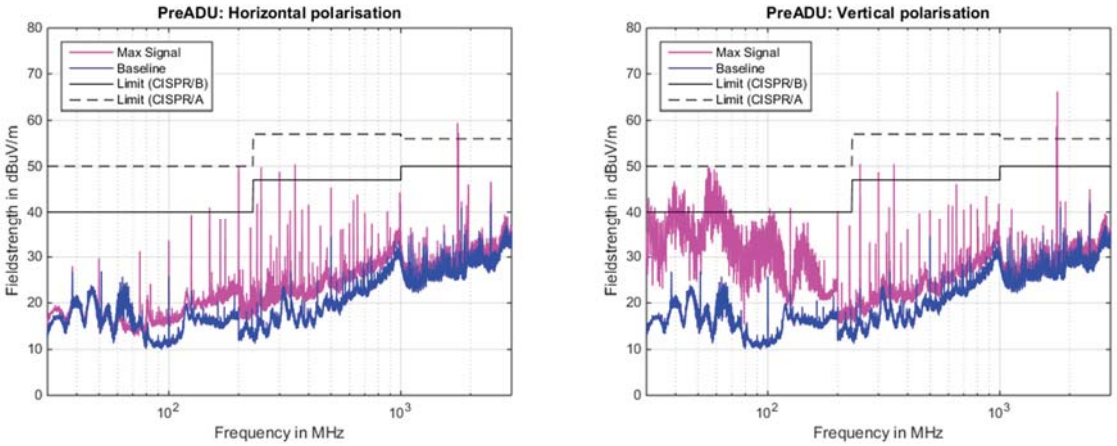


Figure 55. An extract of EMC compliance test results.

5.2 ADU Tests

Some tests have been carried out for the characterization of the first prototype of the ADU board. More specifically, these tests were focused on the performance evaluation of the data acquisition unit of the board, i.e. the ADCs, the analogue network between the input part and the ADCs and their interconnections with the processing sub-system. These tests were important also to evaluate the influence of clock distribution circuit.

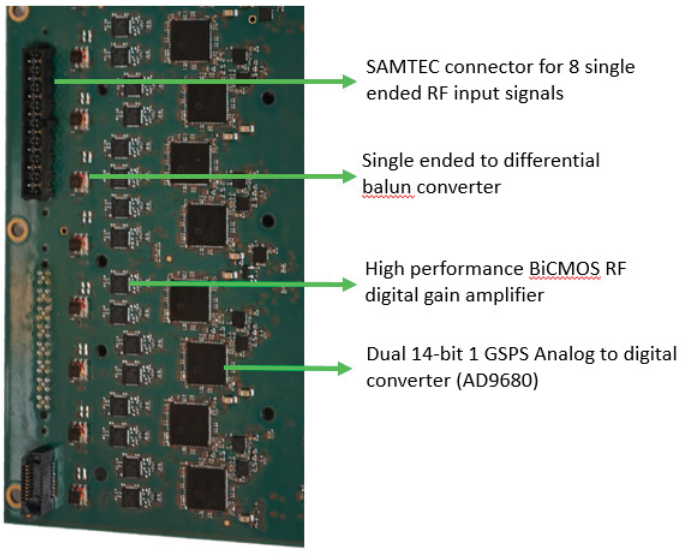


Figure 56. ADU data acquisition unit under test.

As showed in the picture, following the signal path from left to right, the 32 analogue input signals coming from the pre-ADU boards are converted from single ended to differential by baluns, amplified

by programmable Digital Gain Amplifier (DGA) chips and digitized with 14-bit dual-input ADCs that send the 8 most significant bits to the FPGA via high speed serial links for processing.
The ADU integrates in a small sized 6U board a lot of electronics (> 4,000 devices), including 32 ADCs for a wide analogue input data band (up to 500 MHz). So, it was important to verify that the ADU behaviour doesn't get compromised by the presence of 32 ADCs close to each other (e.g. "cross-talk" effect) and no performance degradation is observed. Also, we wanted to evaluate potential undesired effects (e.g. undesirable signals like spurs) generated by the proximity of PCB traces on a high-density board, the proximity of clock signals and the presence of unshielded windings of wire coils of baluns.
As first prototype, two slightly different boards have been manufactured by using the same PCB, corresponding to either a passive or active circuit with the Analog Devices ADA4961 (DGA) chip before each ADC. This allows the amplifiers to be bypassed through a matching network.
Another goal of the tests was the comparison of performances obtained with the two prototypal boards.

5.2.1 Performance evaluation of prototype boards

Two ADU boards (with and without amplifier) have been compared by measuring the performance parameters listed in Table 7. Except for gain flatness (time domain information), these are the typical parameters of dynamic (AC) tests used to characterize the A/D converters and are calculated with a standard Fast-Fourier Transform (FFT) analysis.
Tests are made with the analogue signal at the rated frequency with a signal power of 1 dB below full scale (dBFS) at the inputs of the ADU.
We have adopted the same test procedures used by the High-Speed Converter Group of Analog Devices, Inc., to evaluate high speed analogue-to-digital converters. For more details see [RD7]- [RD9].

Table 7. Performance Parameters.

Gain Flatness [dBFS]	The level of the fundamental tone referenced to full scale.
Signal to Noise Ratio [dB]	The ratio of the rms signal amplitude to the rms value of the sum of all spectral components except the first six harmonics and dc.
Signal to Noise Ratio referenced to Full Scale [dBFS]	The ratio of the rms full scale to the rms value of the sum of all spectral components except the first six harmonics and dc.
Spurious Free Dynamic Range [dBc]	The ratio of the rms value of the signal to the rms value of the worst spurious signal (HD or not) regardless of where it falls in the frequency spectrum.
Harmonic Distortion [dBc]	The level of the first six harmonics referenced to the carrier.
Worst Other Spur [dBc]	The level of the worst spurious component excluding the first six harmonically related components referenced to the carrier.
Total Harmonic Distortion [dBc]	The ratio of the rms signal energy to the rms value of the sum of the first six harmonics.
ENOB [bits]	Effective Number of Bits.
Cross-Talk [dBc]	The measure of any feedthrough coupling onto the quiet channel referenced to the carrier.
Second-Order Intercept Point [dBm] Third-Order Intercept Point [dBm]	$IP_n = P + \frac{\Delta P}{n-1},\ n = 2\ (IP_2),\ 3\ (IP_3)$ where *P* is the output power of the fundamental, and *ΔP* is the difference between *P* and the n^{th}-order Intermodulation Distortion (IMD) product.

For these parameters, the only requirements stated in internal SKA engineering specification documents concern gain flatness (≤ ±1.5 dB), ENOB (≥ 7.5) and cross-talk (≤ 30 dB). Nevertheless, the other parameters were measured as well to have a reference value to be checked during production test in order to assess the good functionality of the produced boards and, in case of problems, possibly find the faults.

We have set up a test bench in Medicina laboratories that includes a signal generator (low phase noise, flat frequency response and reasonable harmonic performance), tuneable band-pass filter, low-pass and high-pass filters, RF power meter, low noise power supplies, a stable reference signal, the ADU board under test and a workstation for instrument control, data acquisition and data analysis.
A comprehensive description of the test set up and methods along with the firmware and software developed to accomplish the measurements of the parameters of Table 7 is reported in [RD10].
Single-tone tests have been performed to calculate the value of gain flatness, SNR, SFDR, HD products, WO spurs, THD, ENOB and cross-talk. Two-tone testing has permitted to measure 2nd-order and 3rd-order IMD products due to ADC nonlinearities. Then we have been able to infer IP2 and IP3 values.
All the results obtained with the measurements executed on the two ADU boards are summarized in Table 8 and Table 9.

Table 8. Comparison of the two ADU Boards in terms of performance parameters in low frequency band.

Performance parameters	ADU Board#1 (with ADA) BW: 50 ÷ 375 MHz	ADU Board#2 (without ADA) BW: 50 ÷ 375 MHz
Single tone analysis		
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 49.2	**≥ 49.3**
Gain Flatness [dBFS]	≤ ±0.4	**≤ ±0.3**
2nd-order Harmonic Distortion [dBc]	≤ -67.2	**≤ -67.7**
3rd-order Harmonic Distortion [dBc]	≤ -66.5	**≤ -68.6**
Worst Other Spur [dBc]	**≤ -67.0**	≤ -66.8
Spurious Free Dynamic Range [dBc]	≥ 66.5	**≥ 66.8**
ENOB [bits]	≥ 7.9	**≥ 7.9**
Cross-Talk [dBc]	**≤ -65.7**	≤ -61.0
Two Tone analysis		
Spurious Free Dynamic Range [dBc]	**≥ 76.3**	≥ 76.0
Worst Other Spur [dBc]	**≤ -77.2**	**≤** -76.0
IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	29.6	**32.2**
IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	66.3	**77.5**

Table 9. Comparison of the two ADU Boards in terms of performance parameters in high frequency band.

Performance parameters	ADU Board#1 (with ADA) BW: 375 ÷ 650 MHz	ADU Board#2 (without ADA) BW: 375 ÷ 650 MHz
Single tone analysis		
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 48.9	**≥ 49.3**
Gain Flatness [dBFS]	**≤ ±0.6**	≤ ±1.4
2nd-order Harmonic Distortion [dBc]	**≤ -65.8**	≤ -59.9
3rd-order Harmonic Distortion [dBc]	≤ -60.8	**≤ -65.6**
Worst Other Spur [dBc]	**≤ -64.2**	≤ -63.2
Spurious Free Dynamic Range [dBc]	**≥ 60.8**	≥ 59.9
ENOB [bits]	≥ 7.8	**≥ 7.9**
Cross-Talk [dBc]	**≤ -70.6**	≤ -70.4
Two tone analysis		
Spurious Free Dynamic Range [dBc]	**≥ 72.0**	≥ 68.3
Worst Other Spur [dBc]	≤ -80.8	**≤ -84.1**
IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	**26.2**	24.4
IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	**64.2**	58.3

The values reported on the tables are relative to the worst case considering all ADU inputs and all frequencies for that measurement. Also, we have highlighted with bold type the best value between the two boards. As can be noticed, the two versions present similar performances.
We can see from the results that ENOB is very high (> 7.8) in all the considered cases and it complies with the requirements. Also, cross-talk and gain flatness levels are within specification.

5.2.1.1 *Firmware tests*

To evaluate the firmware performance, the internal ADU signal generation has been used. This generator substitutes the actual digitized signal with pseudorandom white noise, synchronized among ADUs, and up to 2 sinusoidal tones with prescribed amplitude and phase. The signal from each antenna can be delayed by an integer number of ADC samples to simulate a geometric delay. The beamformed signal is then sent to a software correlator for analysis using the 40 GB Ethernet interface. Several tests have been performed in order to check that the firmware behaves as expected (no closure errors or VHDL synthesis errors are present), and to extend the simulation results to long integration times.

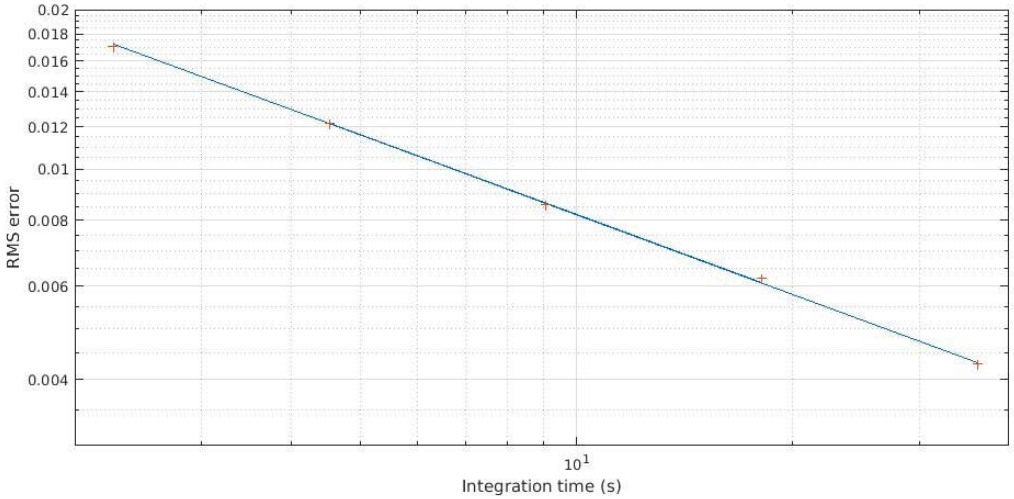


Figure 57. RMS error vs. integration time

Using a white noise signal, reduction of the radiometric noise as a function of integration time has been tested up to 6 minutes. No deviations from the expected $t^{-1/2}$ law was observed (Figure 57).

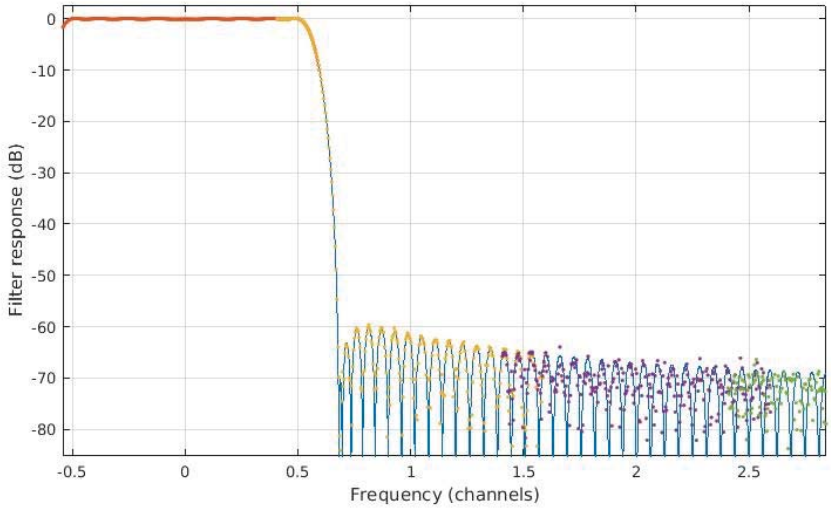


Figure 58. Channeliser response, design vs. measurements

Bandpass and stopband response was tested using a tone plus a weak white noise. Noise is necessary for dithering, to extend the test sensitivity below what is possible using an 8 bit digitiser. Result is shown in Figure 58. The signal amplitude in the channel containing the tone and in the adjacent 3 channels are shown in different colours. Correspondence is very good up to at least -70 dB.

Bandpass response is shown, magnified, in Figure 59.

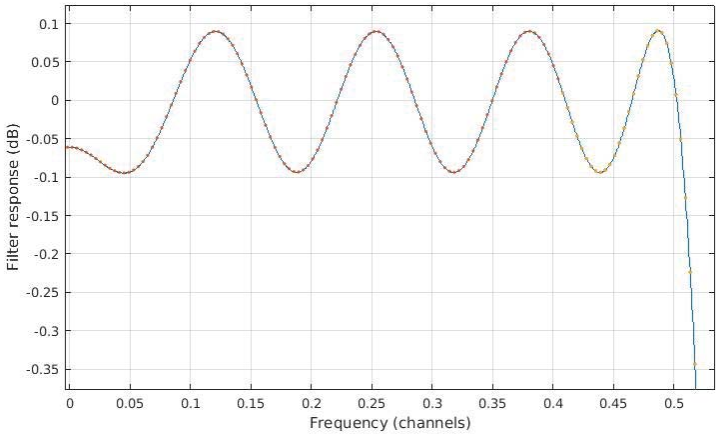


Figure 59. Measured vs. design bandpass response

Beamforming has been simulated by delaying the signals form each antenna in the generator and compensating the delay in the beamformer. Test has been performed both using a monochromatic tone and a pseudorandom white noise. In Figure 59Figure 60 (left) beamforming is performed using

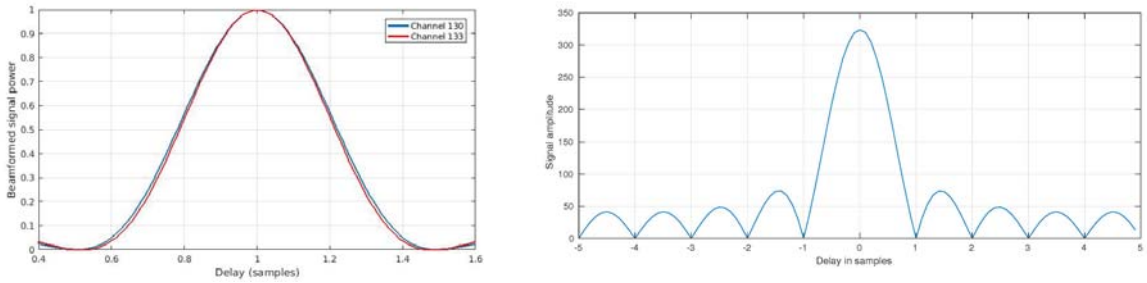


Figure 60. Simulated beamforming. Left: using two tones , right: using white noise

an array of 16 antennas, in a linear array equispaced by 1 sample (1.25 ns), for tone frequencies of 101.56 and 103.91 MHz. On the right, using white noise at 50 MHz.

A sky scansion of the beam has been simulated using the delay rate generator in the FPGA. An example of such a scan, for a linear array of 8 antennas, with a delay range of ±17.5 ns (±5.25 m) is shown in Figure 61. Delay compensation is initially zero and correctly compensates the signal delays after 600 seconds. The input signal is a tone at 101.56 MHz. Since the array is linear and equispaced, beam is periodic and repeats itself.

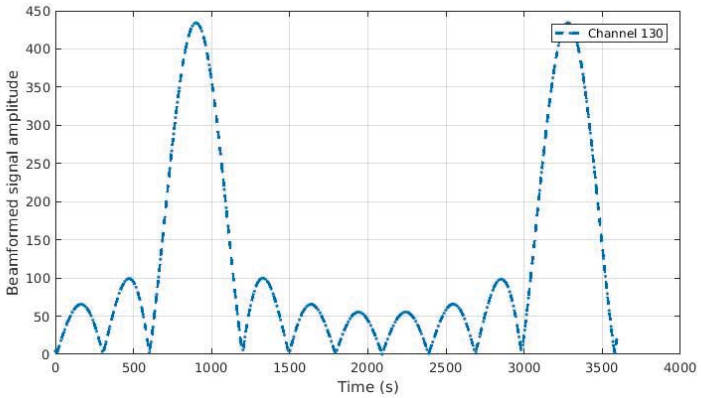


Figure 61. Simulated cross scan of a linear array of 8 antennas. Horizontal axis in seconds

5.2.2 Production tests

5.2.2.1 *RF JIG*

Although AAVS-1 involves a small volume production (about 25 ADU boards for 400 antennas), efforts have been spent towards adopting as much as possible automatic testing procedures.
To this purpose, an RF JIG has been developed. The RF JIG is the TEST board equipment designed to implement the SKA ADU test specification procedure. The RF JIG interfaces with the other test set-up instruments and generates all the analogue stimuli and synchronization signal for the ADU board. The RF JIG main function is to provide a single tone or a two-tone RF signal, generated by an internal or external source, to each TPM-ADU RF input at a time or to all TPM-ADU RF inputs simultaneously. To achieve these two main functions, the board has a common signal conditioning circuit and two separate parallel signal paths, the “switch path” and the “split path”. A picture of the RF JIG is shown in Figure 62.

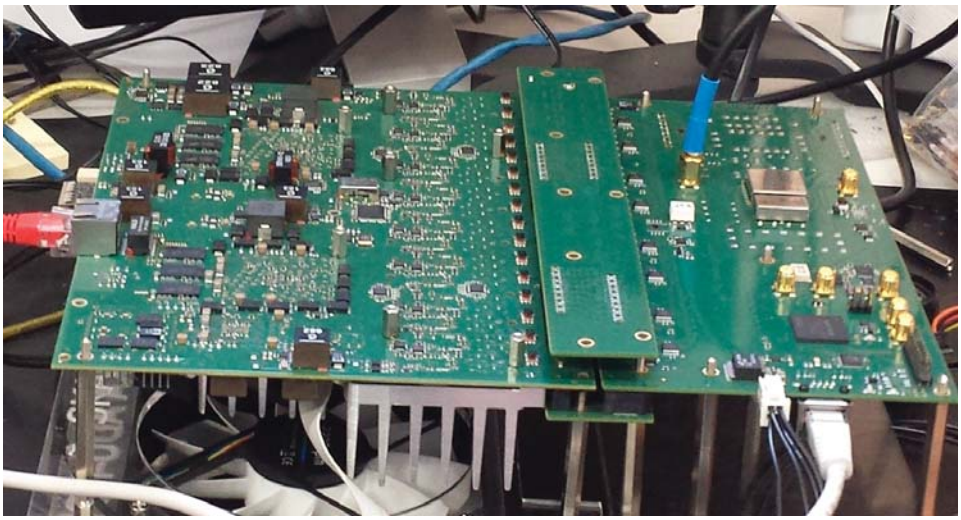


Figure 62. The RF JIG (right) attached to the ADU board (left) during production test. The ADU board is upside down.

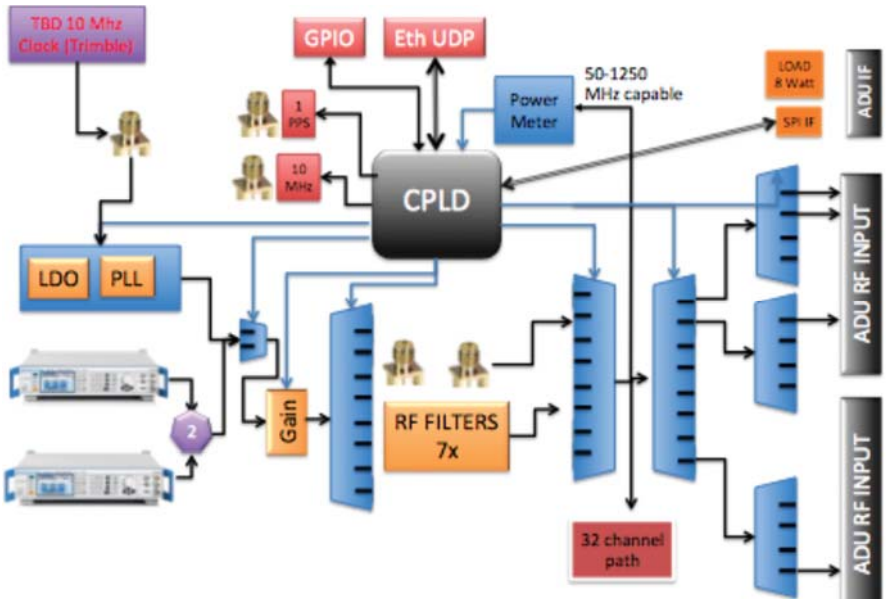


Figure 63. RF JIG signal conditioning and switch path.

All the RF JIG functions are managed by an Ethernet remotely controlled CPLD that configures all the required selection signal and interfaces with the TEST remote application with the bus controlled complex integrated circuits.
The part of the circuit that performs signal conditioning can select two sources of the RF signal. One option is to combine (through power combiner) the signals coming from two external signal generators otherwise the signal is produced by an on board programmable PLL. The PLL can be phase locked with an external ultra-stable reference signal, typically a 10 MHz signal. Internal PLL is present to provide the full functionality without external signal generators. All the PLL circuitry has separate supply that shall be enabled to activate the device.
The selected signal is then amplified and filtered with a SW selectable band pass filter to remove harmonics and sub-harmonics before getting to the RF outputs ports.
After the filter bank the signal power can be measured with a power meter. Knowing the actual power level and controlling the gain stage or the source amplitude for each generated frequency, the signal amplitude can be maintained at a constant target value across frequency. The signal level varies over the bandwidth mainly due to the instability of the source and the differences in the response of the filters.
The signal path is detailed in the following figure with defined expected signal levels.

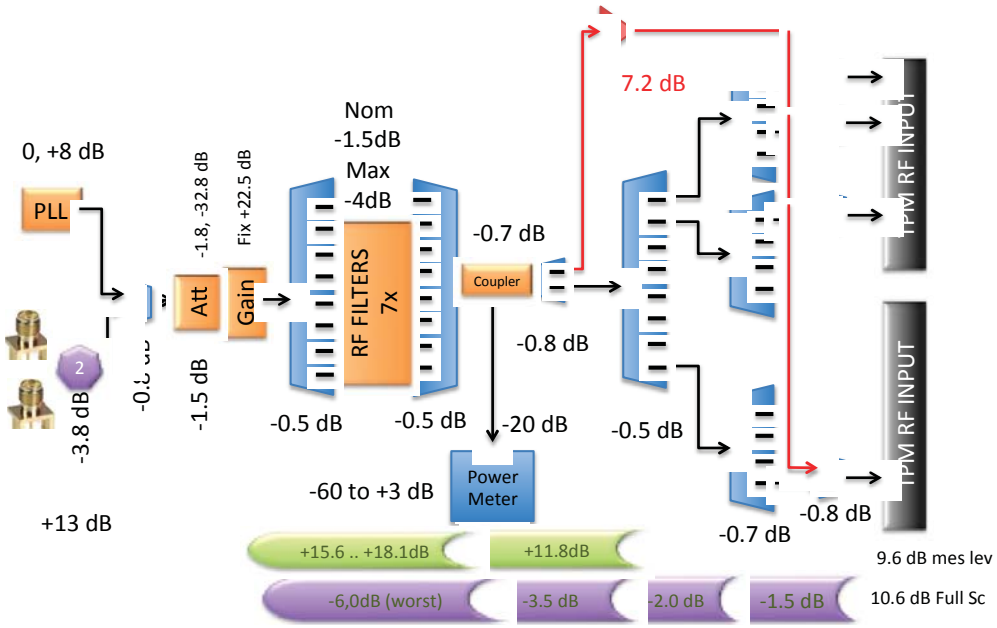


Figure 64. Switch path signal detail.

Because of the large number of passive elements present on each signal path a gain block is required to obtain the desired output signal power.
The required RF performance has been addressed with three main elements:

- high compression point and IP3 components
- tight pass band filters
- high isolation RF switch on the last selection bank (near the output ports)

The RF-JIG on-board switchable filter bank provides a set of seven band pass filters to remove harmonics and out of band noise from the amplified signal before being routed to the output path.
Filter selection has been done with the following criteria:

- Frequency range: from 50 MHz to 1250 MHz

- Frequency step: 12.5 MHz to have 50 steps over the frequency range 50-675 MHz selected for the SKA 1 project.
  For each filter:
- Rejection at 2f > 40 dB (first harmonic)
- Rejection at f/2 ≥ 20dB (first subharmonic)
- In band Insertion Loss ≤ 2.5dB
- In band Return Loss ≥ 15dB.

Filters have been chosen among commercial components. In some cases, a single band pass has been sufficient, otherwise a combination of a low pass and a high pass filter has been necessary to meet the specification.

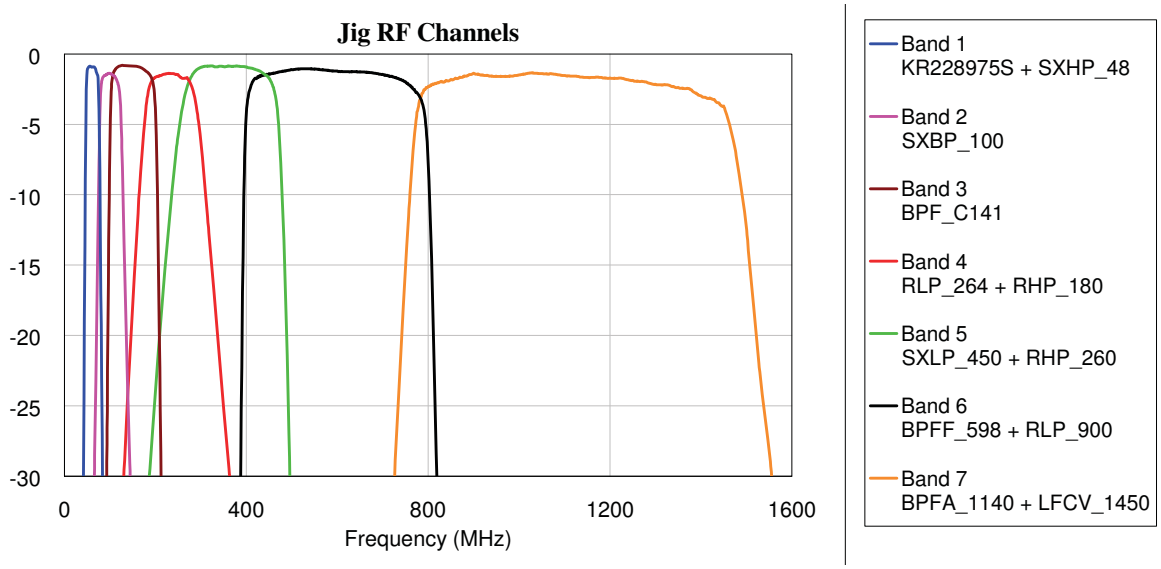


Figure 65. RF JIG Filter bank design.

Once amplified (gain stage), the signal is routed to the appropriate filter controlling the 8-channel switches with the right configuration to let the signal pass to the switch path or the split path.
Further details about the RF JIG can be found in [RD12].

5.2.2.3 *Test procedures*

For the hardware platform verification, the test set-up provides all the capabilities to power the board, configure all the devices of ADU, check temperature, voltages and absorbed power.
It also provides physical and logical connection for all interfaces hosted by the ADU board:

- Power supply connector
- 1 Gbit RJ45 Ethernet interface for the management
- two 40G Ethernet interfaces (QSFP+ connector, optical cable at least 3m length)
- one SMA connector for 10 MHz signal
- one SMA connector for PPS signal
- PRE-ADU interface emulator with ADU ERF8 connector interface.

The 40G Ethernet interface provides the logical link activity and receives data from the ADU at the specified data rate.
The Pre-ADU interface emulator is connected to the corresponding ADU interface and emulates the Pre-ADU load (3.5 V with 2.5 A), the SPI and GPIO digital interface.

To perform the internal bus and the external interface tests, an ADU TEST MODE is defined. It is used for generating pre-defined dynamic test patterns and calculating bus and memory expected maximum error rates (for example, memory test pattern or pseudo-random binary sequence (PRBS) for high speed serial link).
In TEST MODE, a function to download selected ADC test pattern output directly through the 40G Ethernet is also provided.
Specifically, the set of tests foreseen for the ADU board verification is organized as follows:

- Hardware platform verification
  - Check of electrical parameters
    - voltage and impedance
  - Check of configurable board items
  - Check of management functions
  - Check of internal buses
  - Check of external interfaces
  - Check of on-board memories
- RF acquisition quality verification
  - Sampling features
    - Sampling frequencies
    - Phase delay for selected frequencies
  - For each RF-path:
    - Data acquisition over a restricted selected single tone input frequency
- Nominal function verification
  - Check of the firmware version and default values
  - Functional test with full functional firmware for a specified time of continuous operation with:
    - All RF channels and internal functions active
    - All interfaces connected and operating
    - Nominal air flow and environment temperatures
  - Check of all available health parameters
    - Internal voltages
    - Power consumption
    - Temperatures.

Further details on the ADU test plan and procedures for the hardware platform verification can be found in [RD13] and [RD14]. Test report for ADU 1.2 boards is provided in [RD40]. A few ADU boards have been manufactured and tested in The Netherland at ASTRON; the correspond test report is given in [RD41].
The procedure followed to test the RF interface is very similar to that used for performance evaluation in Section 5.2.1. The use of RF JIG makes all the operations highly automated. A stable 10 MHz reference signal is applied to both the ADU and the signal source (external signal generator(s) or RF JIG PLL) so that the ADU is synchronized with the selected signal generator. As mentioned before, the RF JIG provides a good quality analogue signal to the ADU RF inputs. The applied RF signal can be tuned in the 50-650 MHz frequency range, with low phase noise and much attenuated harmonics contribution (thanks to filter bank in RF JIG).
The RF TEST procedure allows to apply one power-controlled RF signal at each ADU input at a time with the others terminated to 50 Ohm load. The RF signal measured at the selected ADU board input must always have a constant level of about -1 dBFS over the bandwidth. The RF TEST method offers

also the possibility to apply simultaneously the same RF signal to all the ADU inputs with a passive equalized path.
A block diagram of the TEST set-up is sketched below.

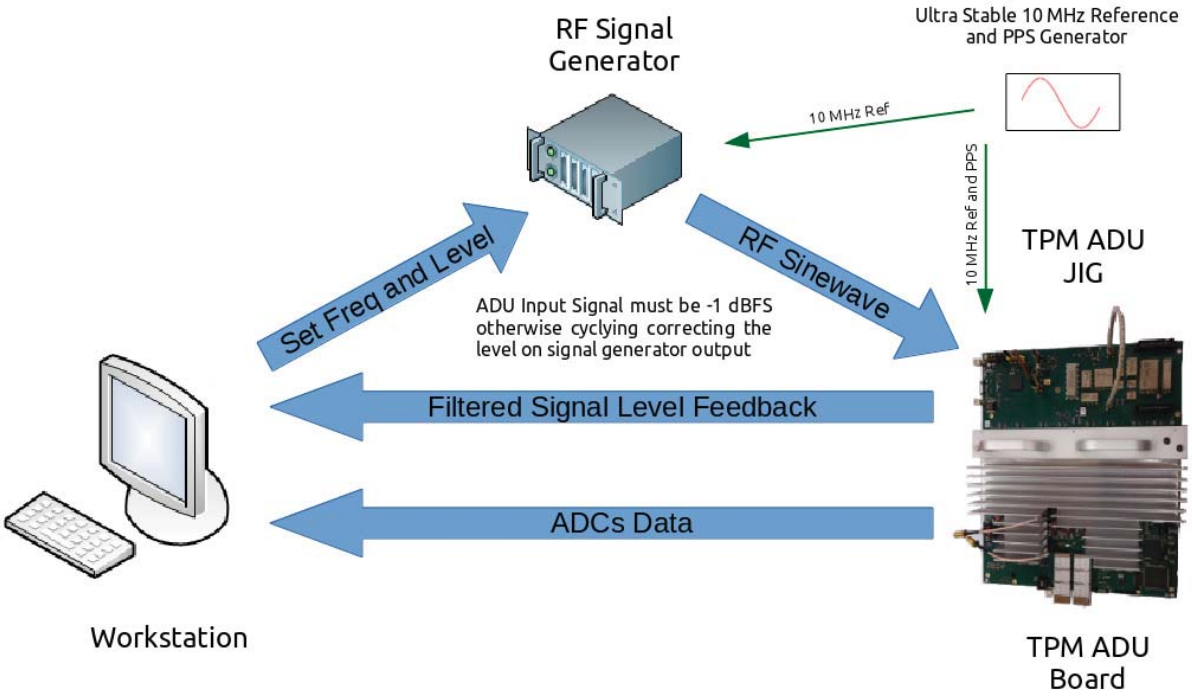


Figure 66. RF TEST set-up block diagram.

The workstation sets frequencies to the signal generator and corrects the amplitudes by reading the level measured by the calibrated power meter (of the RF JIG).
When in RF TEST MODE, the ADU board can provide the following functions:

- send over the 40 G Ethernet interface or the 1G management link $2*10^6$ samples of contiguous time-domain data from one selected RF input
- send over the 40 G Ethernet interface or the 1G management link $256*10^3$ samples of contiguous and simultaneous time-domain data from eight selected RF inputs
- send over the 40 G Ethernet interface or the 1G management link $64*10^3$ samples of contiguous and simultaneous time-domain data from all RF inputs.

These capabilities are available for all the ADU sampling frequencies.
The workstation collects data from the ADU board through the 40G Ethernet interface or the 1G management link without packet loss.

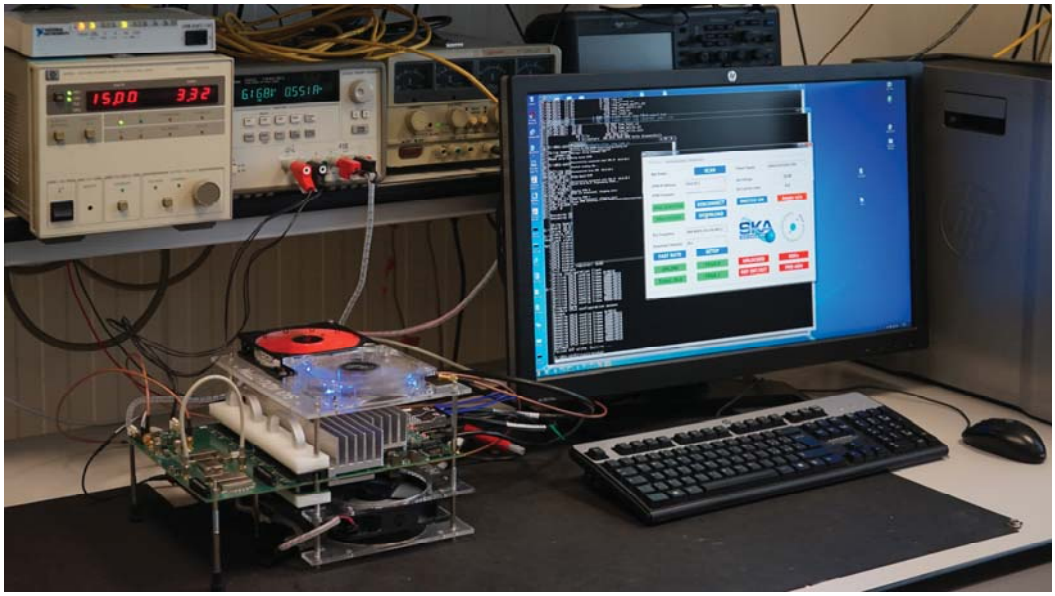


Figure 67. The test bench used during production tests.

Once time-domain data are saved into files a MATLAB application performs the data analysis calculating all the parameters of Table 7. Also, it permits the generation of useful plots and the final test report that includes a table with all the results specifying if the board under test is compliant with the specification or not. For this software we have created a graphical user interface (GUI), as showed in Figure 68.

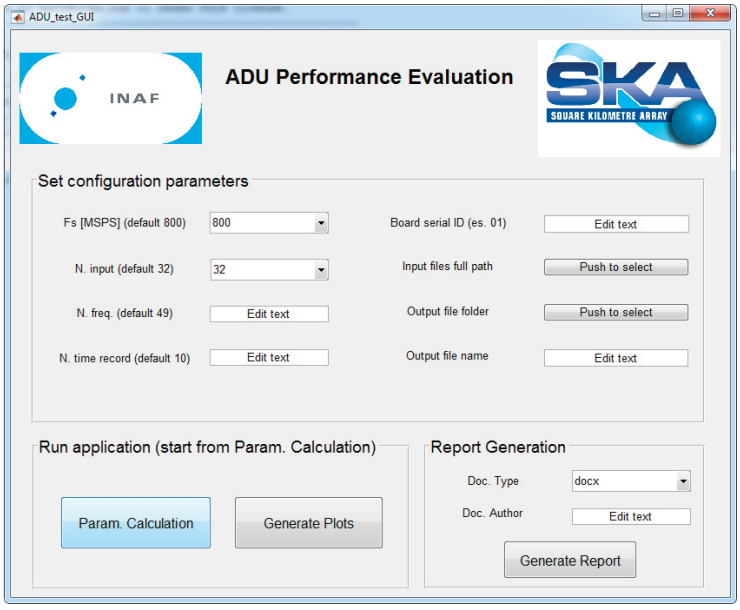
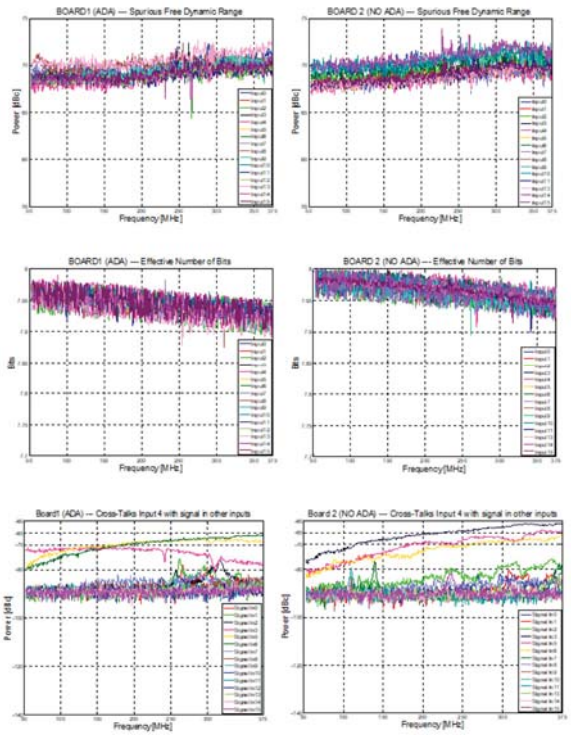


Figure 68. GUI of the MATLAB application used for ADU performance evaluation during production tests.

An example of performance test report along with some plots of the principal evaluation parameters is reported in the next figure.



INAF

Author INAF
Measure Date 2016-11-22
Report Date 2016-11-23

ADU Board ID	1.2.5041602002
Frequency	50 - 375 MHz

	SNRFS [dBFS]	Gain Flat. [dBFS]	HD2 [dBc]	HD3 [dBc]	WO [dBc]	SFDR [dBc]	ENOB [Bits]	Cross-Talk [dBc]	TEST
In0	48.97	0.65	-80.21	-66.92	-63.16	63.67	7.86	-51.95	PASS
In1	48.91	0.70	-78.98	-67.26	-63.07	63.64	7.87	-50.41	PASS
In2	49.01	0.64	-80.37	-66.12	-64.42	64.76	7.86	-51.23	PASS
In3	49.07	0.70	-78.31	-66.12	-64.43	64.99	7.86	-49.43	PASS
In4	49.02	0.68	-74.44	-67.22	-65.13	65.62	7.87	-51.91	PASS
In5	49.05	0.60	-74.08	-64.93	-65.10	65.70	7.90	-52.10	PASS
In6	49.11	0.73	-74.76	-69.06	-65.07	65.56	7.87	-53.90	PASS
In7	49.10	0.66	-74.70	-68.38	-64.92	65.43	7.87	-67.78	PASS
In8	49.07	0.64	-70.48	-67.27	-64.75	65.38	7.88	-64.06	PASS
In9	49.06	0.70	-71.10	-64.51	-64.62	65.09	7.88	-54.92	PASS
In10	49.13	0.57	-70.72	-65.89	-64.46	64.85	7.89	-51.17	PASS
In11	48.97	0.48	-70.40	-63.93	-64.21	64.78	7.84	-58.17	PASS
In12	48.98	0.63	-77.64	-69.55	-63.86	64.44	7.89	-53.75	PASS
In13	49.00	0.60	-76.92	-63.81	-63.96	64.41	7.87	-60.36	PASS
In14	49.03	0.65	-76.91	-67.61	-63.32	63.91	7.88	-54.74	PASS
In15	48.97	0.56	-75.87	-68.63	-63.14	63.60	7.84	-71.93	PASS
In16	49.03	0.64	-74.28	-69.32	-64.36	64.95	7.88	-66.99	PASS
In17	49.02	0.66	-75.47	-65.92	-64.37	64.87	7.86	-65.47	PASS
In18	49.10	0.71	-77.12	-66.85	-65.22	65.64	7.86	-56.27	PASS
In19	49.00	0.59	-81.04	-65.72	-65.22	65.73	7.86	-48.12	PASS
In20	49.21	0.72	-73.09	-69.61	-66.15	66.57	7.88	-54.71	PASS
In21	49.16	0.75	-72.47	-67.89	-66.13	66.63	7.90	-51.99	PASS
In22	49.07	0.65	-77.14	-68.29	-66.09	66.47	7.88	-59.43	PASS
In23	49.19	0.62	-71.14	-71.78	-66.02	66.45	7.88	-57.04	PASS
In24	49.09	0.88	-73.90	-67.76	-66.10	66.74	7.90	-53.02	PASS
In25	49.03	0.78	-72.90	-68.98	-66.12	66.66	7.90	-59.19	PASS
In26	49.07	0.68	-74.14	-68.86	-66.09	66.49	7.88	-55.12	PASS
In27	49.12	0.64	-76.02	-65.69	-65.98	66.50	7.91	-51.08	PASS
In28	49.01	0.71	-79.70	-66.76	-64.63	65.15	7.85	-53.70	PASS
In29	49.08	0.64	-79.62	-68.57	-64.96	65.40	7.89	-53.47	PASS
In30	48.89	0.59	-80.70	-69.06	-64.10	64.58	7.86	-54.49	PASS
In31	48.93	0.48	-80.35	-67.58	-64.27	64.84	7.88	-64.02	PASS

Figure 69. Example of the ADU performance test report with plots and table.

5.2.3.3 Integration test

The TPMs have been mounted (1 ADU board + 2 Pre-ADU boards) at the Medicina Integration Test Facility (ITF). They have been tested to check again performance parameters as a checkout test before to be shipped to Australia.



Figure 70. An integrated TPM (left) and a TPM front Panel (right).

Since the TPM accepts only analogue optical signals, the test was done using a spare Front End TX to inject a single tone sinewave of amplitude level -60 dBm (one different frequency per RF input) per

TPM input polarization (as shown in next picture), one TPM input at time. The signal level measured by the ADCs is expected to be around 0 dBm (for about 60 dB of gain).

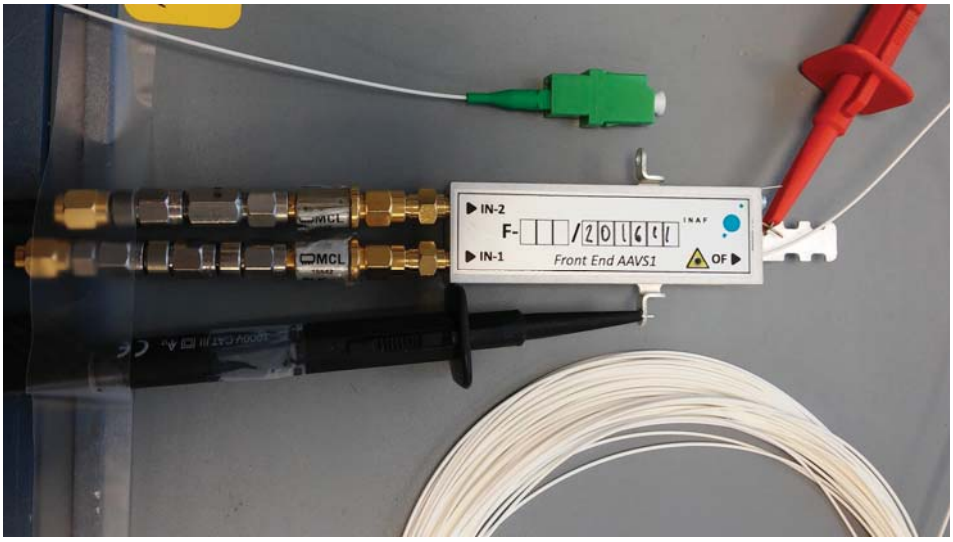


Figure 71. A spare Antenna Front End Tx used to inject two optical sinewaves to measure TPM input performance after integration.

The test keeps record also of the board temperatures within the Sub-racks (working at room lab temperatures).



Figure 72. A TPM Sub-rack under test.

There are test reports for each TPM board showing the performances.

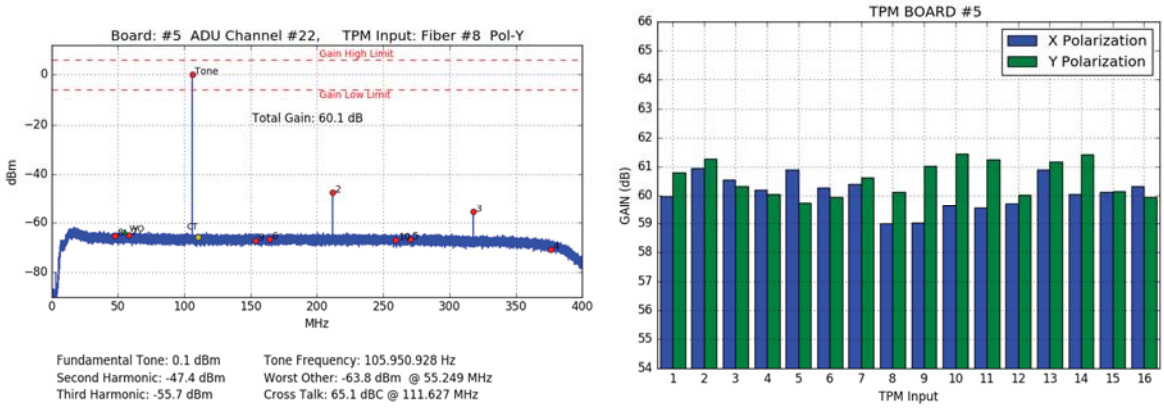


Figure 73. Example of results of a TPM after integration.

Then the TPMs are now ready to be packed for the AAVS1 shipment.



Figure 74. TPMs integrated and tested ready to be packed and shipped to Australia.

5.2.4 TPM on site test

The TPMs shipped to Australia have been tested for EMC measurements by ICRAR using the CISPR/B level requirements and all of them passed the test (see next two pictures) [RD6].

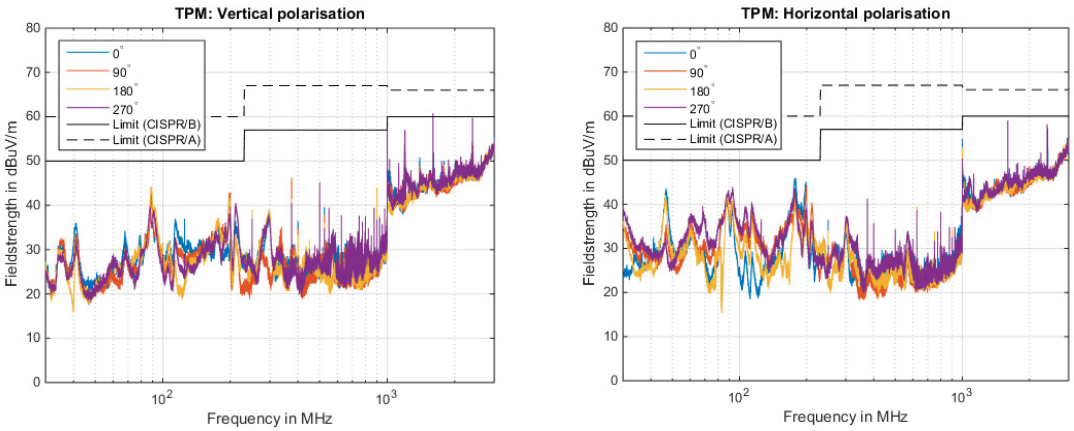


Figure 75. A sketch of the Sub-rack EMC test results.

Then the TPMs have been shipped to MRO and a quick performance test of each board has been repeated to verify that the shipment did not affect functionality and performances.

A dedicated optical signal generator has been designed to output 4 tones. This 1U rack mountable box is used to test TPM performances and both synchronization between FPGAs of the same board or synchronization between TPMs of the same Rack/Sub-rack.

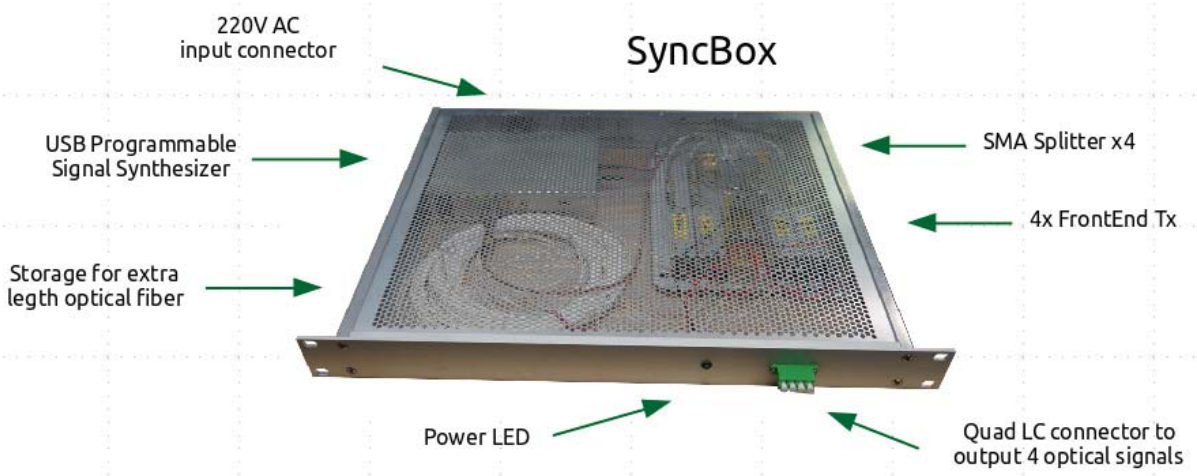


Figure 76. The SyncBox shipped to Australia to test performance of TPM on site.

5.2.5 AAVS1 Installation test

The AAVS1 on field installation [RD42] requires a dedicated software and TPM FPGA firmware to get fast responses measuring the performance of the antennas without importing the heavy station access layer of the telescope management software.

The performance of the complete system (antenna+LNA+optical Tx/Rx+fibers+TPM) is tested by looking at the shape and the power of spectra comparing the spectrum of a reference antenna deployed on the AAVS site months before.

A careful data analysis allows the user to identify the source of the issue which may be related to one or more parts of the system. A user shared log file based on a google spreadsheet keeps track of each issue and the fix applied.

Two software have been developed to:

1. Manage TPMs on Sub-racks
2. Make some quick data analysis

The TPM management software is written in Python language using Qt4 libraries to provide a GUI.

TPMs are grouped by sub-racks, an xml file for each sub-rack provides information on how to connect to a TPM and ADU and Pre-ADUs serial numbers.



Figure 77. TPM's sub-rack management software.

The software shows the status of each TPM in the sub-rack, such:

- if FPGAs are programmed and which firmware is running
- ADCs sample rate and synchronization info
- status of Pre-ADU (on/off)
- board temperatures
- status of connection (online/offline)



Figure 78. TPM's Sub-rack Status as shown by the software

It is possible to enter to the Pre-ADU configuration by clicking on the Pre-ADU status label and read the configuration or changed by both editing numbers and pushing buttons for:

- set a value for each digital step attenuator of each input signal
- select the filter of the band
- terminate to 50ohms the input signal

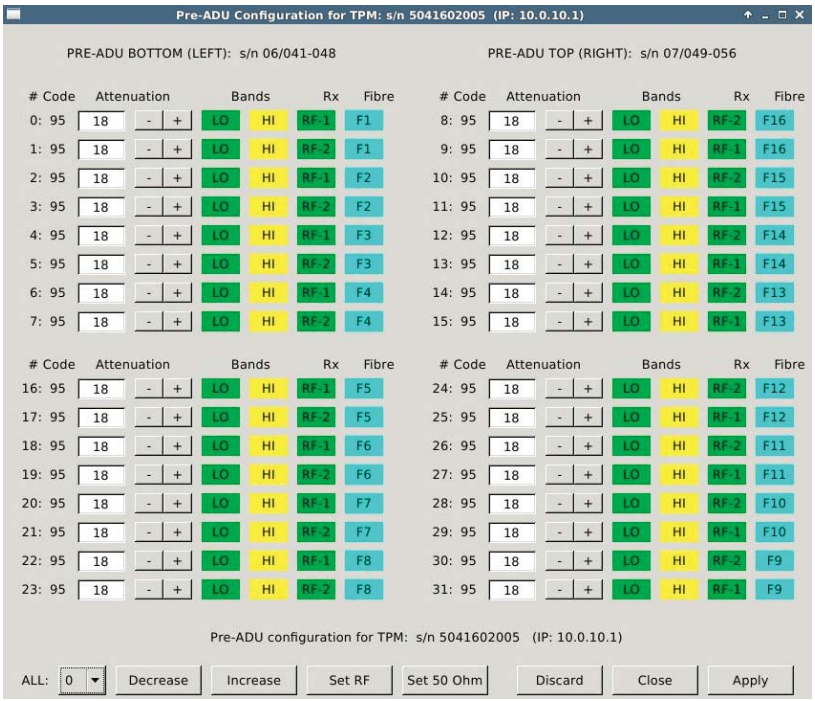


Figure 79. Pre-ADU setup window.

The data analysis software is written in Python and provides a GUI as well and it is showed in the next picture.

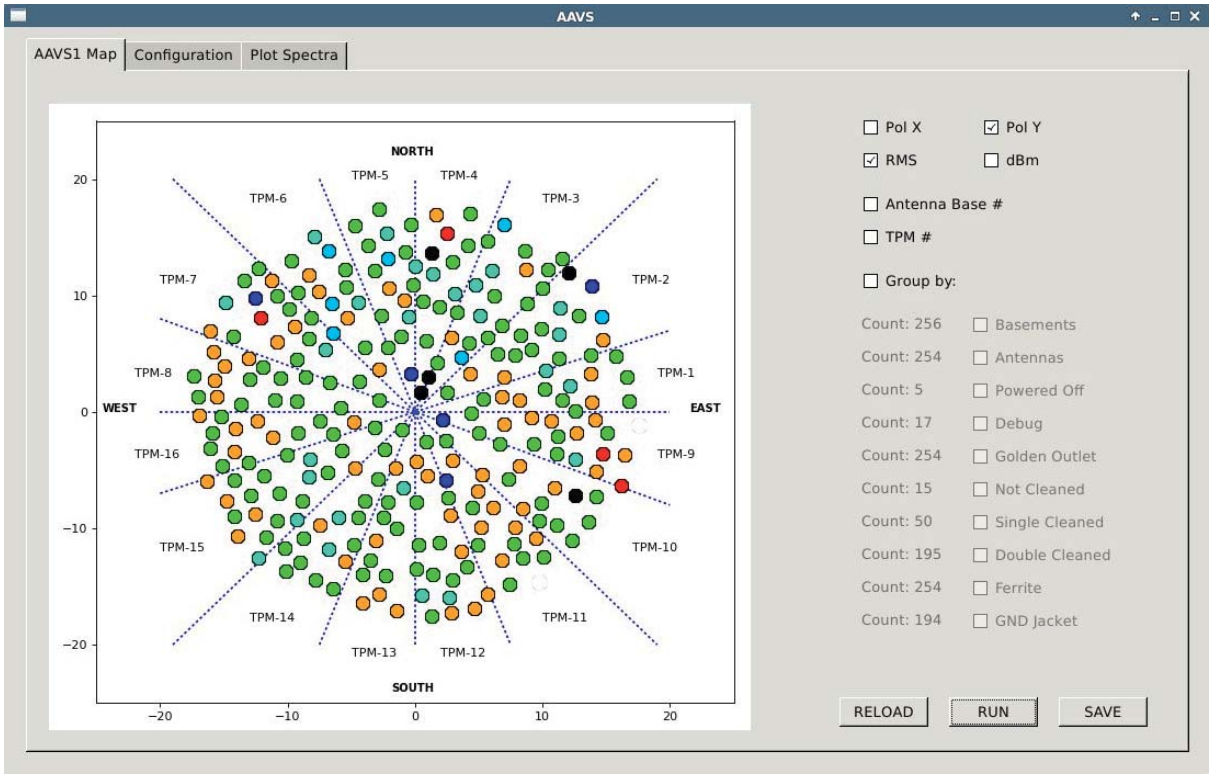
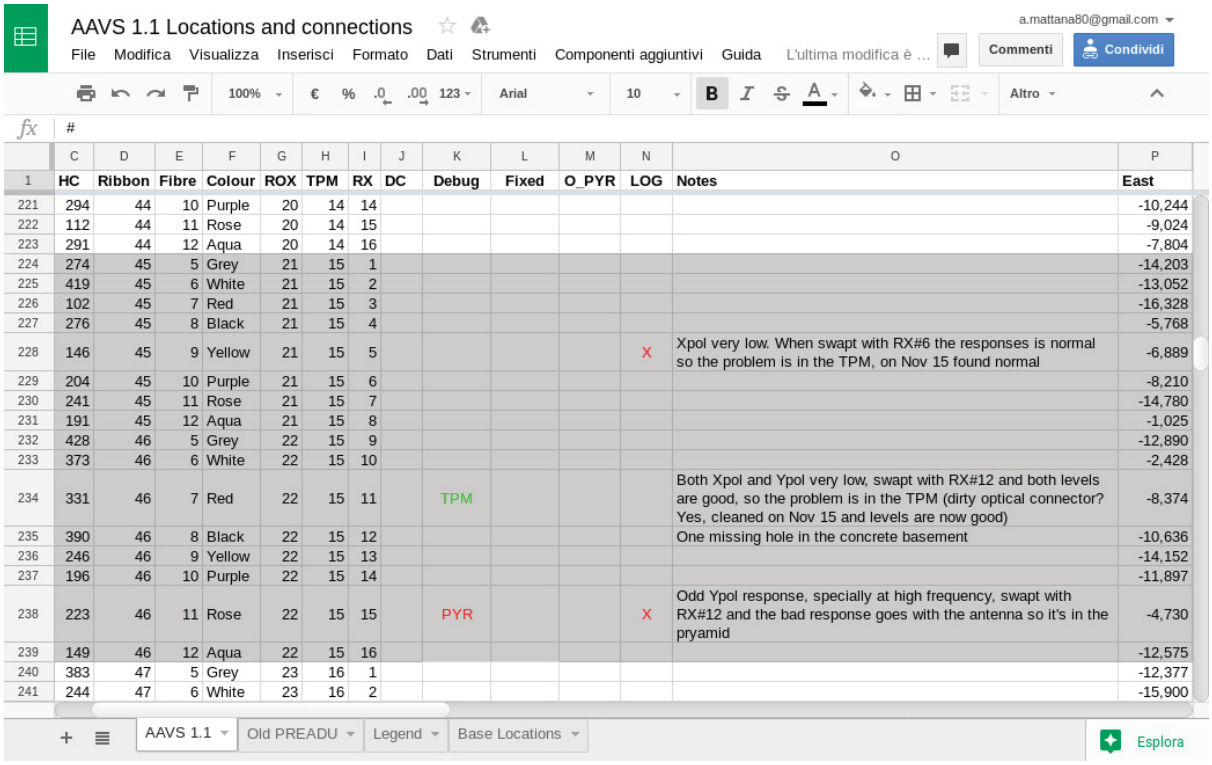


Figure 80. AAVS1 Tile installation software.

When started it looks for the google spreadsheet containing the antennas position to generate the map of the array. Each antenna record on the spreadsheet contains:

- Antenna Sequence number
- Antenna Basement number
- Hybrid Cable number
- Ribbon Number
- APIU Fibre number
- Fibre Colour
- APIU Roxtec Input number
- the TPM number (last part of the IP address) in which the antenna is connected
- the number of the TPM input in which the antenna is connected
- status of the LNA power supplied by the APIU (on/off)
- the antenna position relative to the centre of the array (east/north)
- Debug status plus comments
- Flags saying what kind of bug fixing has been applied (Hybrid cable outlet, ferrite, single/double cleaning from rust, FE ground jacket)



	C	D	E	F	G	H	I	J	K	L	M	N	O	P
1	HC	Ribbon	Fibre	Colour	ROX	TPM	RX	DC	Debug	Fixed	O_PYR	LOG	Notes	East
221	294	44	10	Purple	20	14	14							-10,244
222	112	44	11	Rose	20	14	15							-9,024
223	291	44	12	Aqua	20	14	16							-7,804
224	274	45	5	Grey	21	15	1							-14,203
225	419	45	6	White	21	15	2							-13,052
226	102	45	7	Red	21	15	3							-16,328
227	276	45	8	Black	21	15	4							-5,768
228	146	45	9	Yellow	21	15	5					X	Xpol very low. When swapt with RX#6 the responses is normal so the problem is in the TPM, on Nov 15 found normal	-6,889
229	204	45	10	Purple	21	15	6							-8,210
230	241	45	11	Rose	21	15	7							-14,780
231	191	45	12	Aqua	21	15	8							-1,025
232	428	46	5	Grey	22	15	9							-12,890
233	373	46	6	White	22	15	10							-2,428
234	331	46	7	Red	22	15	11		TPM				Both Xpol and Ypol very low, swapt with RX#12 and both levels are good, so the problem is in the TPM (dirty optical connector? Yes, cleaned on Nov 15 and levels are now good)	-8,374
235	390	46	8	Black	22	15	12						One missing hole in the concrete basement	-10,636
236	246	46	9	Yellow	22	15	13							-14,152
237	196	46	10	Purple	22	15	14							-11,897
238	223	46	11	Rose	22	15	15		PYR			X	Odd Ypol response, specially at high frequency, swapt with RX#12 and the bad response goes with the antenna so it's in the pryamid	-4,730
239	149	46	12	Aqua	22	15	16							-12,575
240	383	47	5	Grey	23	16	1							-12,377
241	244	47	6	White	23	16	2							-15,900

Figure 81. Google Spreadsheet containing the log of each antenna.

The software allows the user to plot the array map decorating with some extra markers/colours to answer to the query selection such:

- Print antenna basement number, useful to identify an antenna on the map;
- Colour the antenna basements to understand to which TPM the antenna is connected to;
- Colour the antenna basements using a “rainbow” colour-map showing the measured RMS (or power in dBm) of each one, useful to find faster which antenna has low/high signal;
- Highlight antennas that satisfy the query selection (which antenna has a ferrite, has been fixed, is powered off, and so on…) either choosing one of the proposed features or combining some of them.

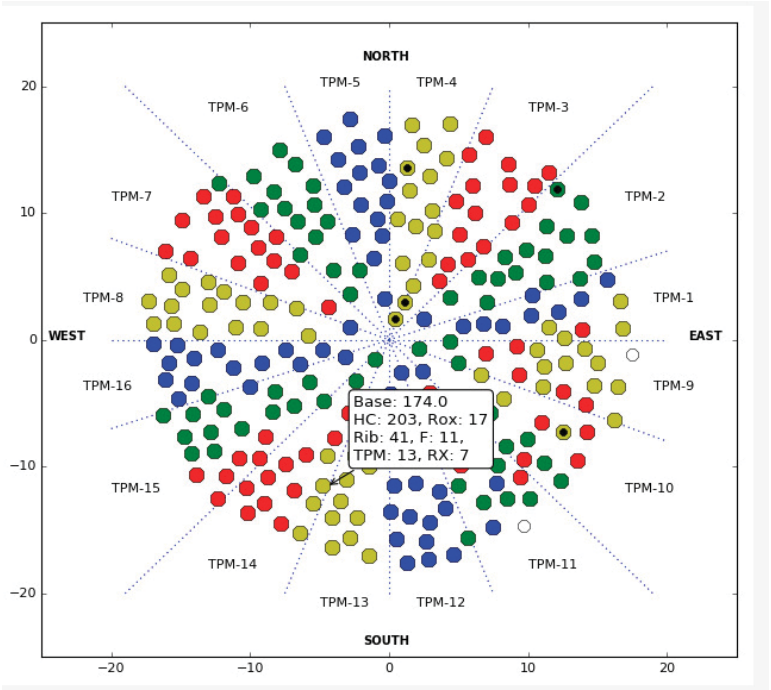


Figure 82. Example of a coloured map meaning which antenna is connected to a TPM. The tooltip popup is shown when moving mouse cursor over an antenna: Base: antenna basement number, HC: Hybrid cable, Rox: Roxtec input, Rib: Ribbon, F: Fibre number, TPM: TPM number. Black dotted antennas are powered off, while there are no antenna mounted on white basements.

The software allows the user to create and save lists of antennas to be plotted for data analysis. It is possible to select a colour to be used for each antenna. The list view shows also the antenna info and status flags.

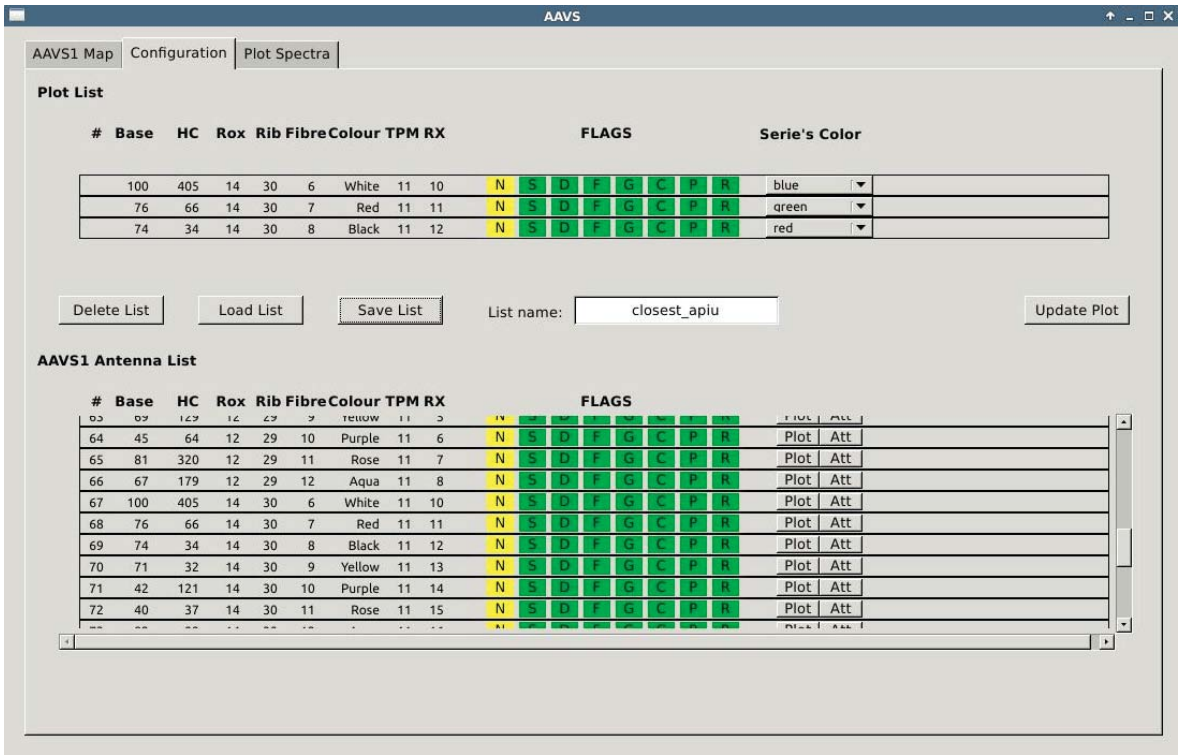


Figure 83. Generating a list of antenna to be plotted.

The last tab of the widget shows the antenna spectra plot. Depending on the selection of the user, this can be a single plot overlaying spectra of the selected polarisation or it can be a multi-plot drawing a plot for each antenna spectrum of the two polarizations.

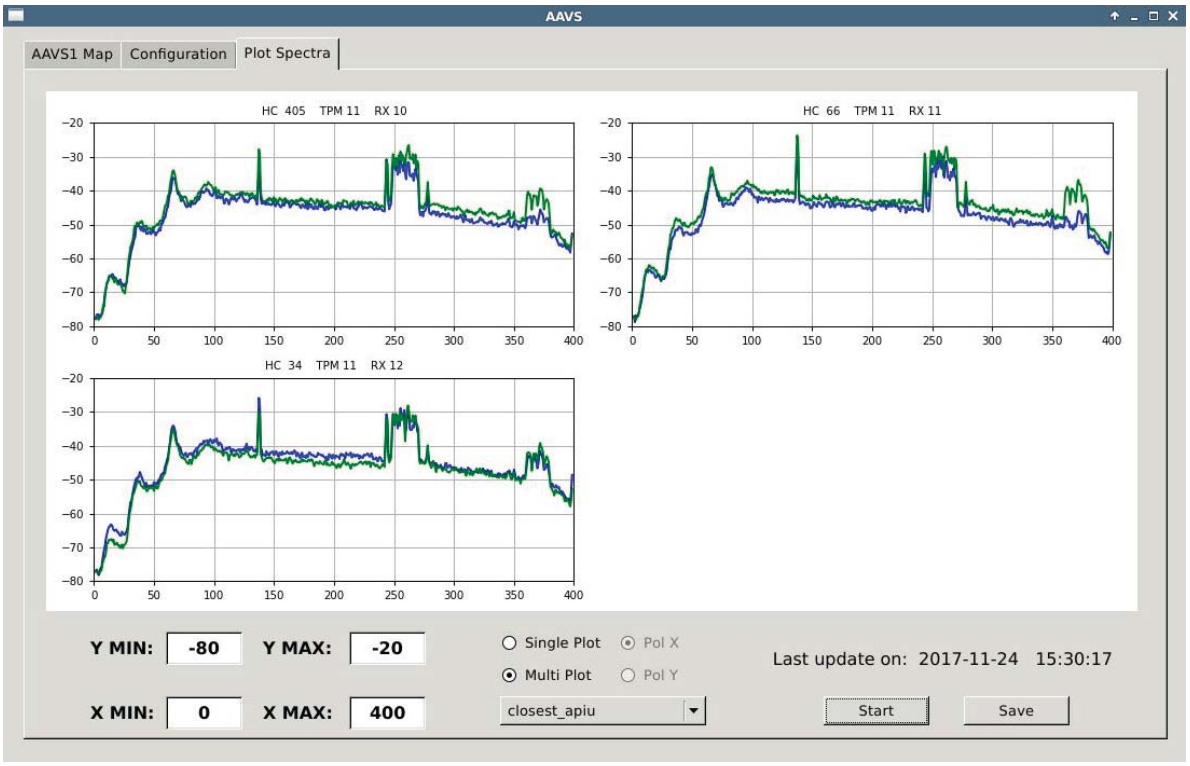


Figure 84. Example of plots of an antenna list.

5.2.6 AAVS1 Night Monitor

When one or more AAVS Tiles have been setup during the day, it is very important to monitor continuously during the night the antennas when there are no workers around the AAVS field.

A dedicated software acquires spectra every 5 minutes to verify if there are some unexpected occasional events and to measure how the level of the signal change along the night. Then each morning before to start continuing the construction activity, the data is checked quickly watching a movie that shows how the antenna spectra change over time. The output will inform the construction team if there are antenna that must be fixed.

5.2.7 AAVS1 Firmware Tests

Several tests have been performed in the lab and on site to evaluate the AAVS1 Firmware, these tests include LMC data generation tests, BER test and DSP firmware tests.

5.2.7.1 *LMC data generation tests*

LMC data generation tests are aimed to verify that the FPGAs transmits data to the LMC as expected. LMC Data formats include raw ADC, channelized and tile beamformed data in addition to the data

generated by the integrated spectrometers which are transmitted to the LMC as well. The FPGA supports the generation of synthetic data at different stage of the processing pipeline defined by a data pattern that can be downloaded to the FPGA. The data pattern substitutes the actual data along the pipeline and is processed identically by downstream modules. Using the data pattern, it is possible to verify the LMC data packets checking for expected data. In case of integrated data processed by spectrometer, the same calculation starting from the pattern data can be performed off-line.

5.2.7.1 *Bit Error Rate Tests*

BER Tests have been executed to evaluate the quality of the ADU Ethernet links. The first test makes use of a packet generator and packet checker which are both associated to each lane of both 40G links supported by the ADU. Software can program the packet generator to transmit test packets to a specific MAC address. The 40G Ethernet switch is then used to forward the transmitted packets to a packet checker addressed by the related MAC address. The received packet is then checked at wire-speed and inconsistency detected permitting to use the full Ethernet bandwidth. The test has been ran for several days without detecting any error; this corresponds to BER < 10^{-15} which represents the specification provided by the manufacturer for the copper cables connecting the ADUs to the 40G Ethernet switch.

A second BER test consists in using the station beamformer infrastructure to process synthetic tile data generated identically by each ADU such that the resulting station beam is equal to the generated synthetic data multiplied by the number of ADUs in the station beamformer chain. The station beam can be directed to the LMC server and checked for errors.

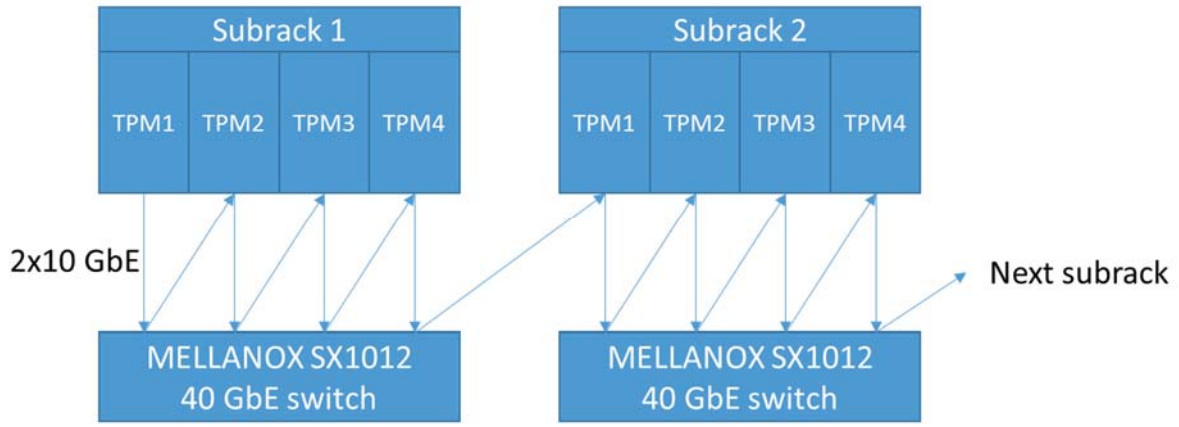


Figure 85. Station beamformer BER test.

5.2.7.2 *Synchronization Test*

This test is aimed to verify the synchronization of ADUs across different sub-racks. The ADUs use the reference clock to generate the ADC sampling clock and sample the PPS to synchronise the acquisition of the data from the ADCs. When different ADUs are synchronised correctly an external reference signal forwarded to one or more ADC inputs is sampled with a phase difference which is consistent across ADU re-initializations. On site the external reference signal is provided by the synchronization box described in section 5.2.4 and forwarded to 4 ADUs. In order to check for the expected behaviour, the following operations are executed in a loop:

- Program and initialise ADUs
- Request LMC channelized data to the ADUs; this result in synchronised data from each ADU being sent and acquired on the LMC server
- Process the acquired data by building the time series for the frequency channel containing the synchronization signal fundamental frequency
- Correlate the time series acquired from one ADU with the other ADUs processing the reference signal
- Calculate delay difference between correlated signals

Repeating the above steps in a loop should always result in a consistent delay difference; in case of synchronisation errors, the data from one or more ADUs would be affected by additional delays in multiples of the sampling period.

5.2.7.4 *Coefficients synchronisation test*

The tile beamformer applies calibration and pointing coefficients to the processed data. These coefficients are updated during an observation and applied synchronously to the data across different ADUs. This test is aimed to verify that the synchronisation mechanism works as expected and coefficient are applied at the same time across multiple ADUs.

The test setup consists in forwarding an external reference signal to several ADUs and acquiring the generated station beam. LMC issue a command to the station to apply new calibration or pointing coefficients while still acquiring the station beam. After the application of the new coefficient, the acquisition of the station beam ends and acquired data are processed offline. Power and phase of the channel containing the reference signal fundamental frequency is then plotted against time. In case the coefficients are applied synchronously across multiple ADUs, the power and phase change abruptly from one steady state to the next one with no intermediate power values between them. On the contrary, when a delay in the coefficient application exists in at least one ADU, the phase and power assume intermediate values between the two-steady states for a number of samples that is related to the delay.

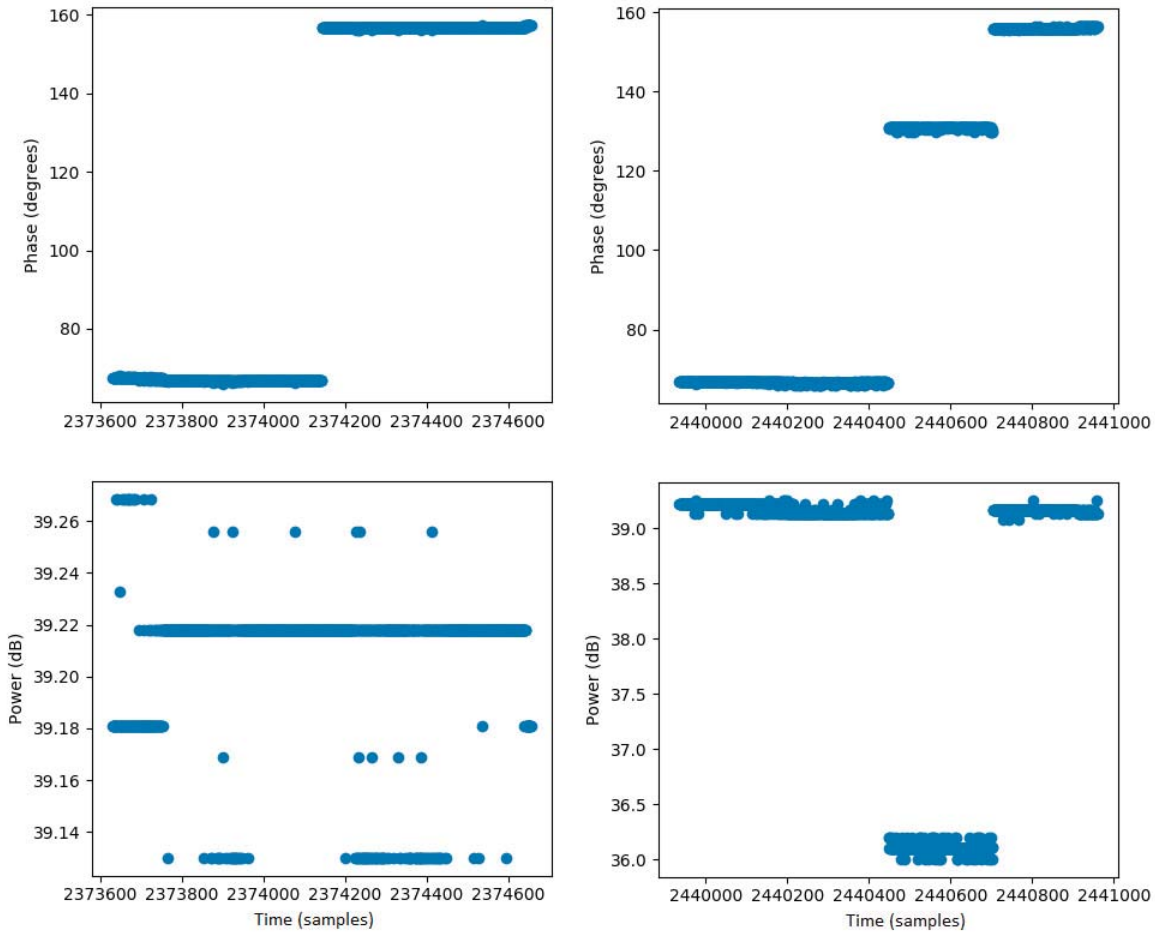


Figure 86. Pointing delay synchronisation. In the left half, application of new coefficients results in a single discontinuity in the beam phase and unaffected power. In the right half a delay in the application of the coefficients has been introduced in one TPM, this results in intermediate power and phase values.

Figure 86 shows an example plot for pointing delay test. In the left half of the figure it is possible to note that the application of the new pointing coefficients doesn't change the power of the station beam, but affects its phase, with the phase changing from one steady state to the next one with no intermediate phase values. In the right half of the figure, an artificial delay has been introduced in the application of the coefficients on one ADU. In this case, power and phase assume intermediate values.

5.3 Thermal/Mechanical

To validate the modelling technique a CFD model of the hardware which was used for the thermal tests at INAF was constructed to compare calculated with measured values.

The hardware is illustrated in Figure 87. The ADU board, 2 x Pre-ADU boards, a side plate and an air deflector were installed at each of the 4 TPM positions in the sub-rack. A drawer with 6 fans below the sub-rack provided the airflow. EMC screens (perforated plates) at the top and bottom of the sub-rack allow the passage of air. Air entered the fans at 25°C. Temperatures were monitored at a point on the ADU PCB.
The AAVS1 thermal model is illustrated in Figure 88.

In the ANSYS Icepak/Fluent model the TPM assembly was moved across the sub-rack giving the solutions identified by positions 1, 2, 3 and 4 in Figure 87 below. Pictures from Figure 89 to Figure 92 are plots of the airflow for each of the four positions. For the simulation nominal design values of 25 W and 3 W were used for the FPGAs and ADCs power dissipation respectively. For each of the PRE-ADU boards the measured value of 9.3 W was used.

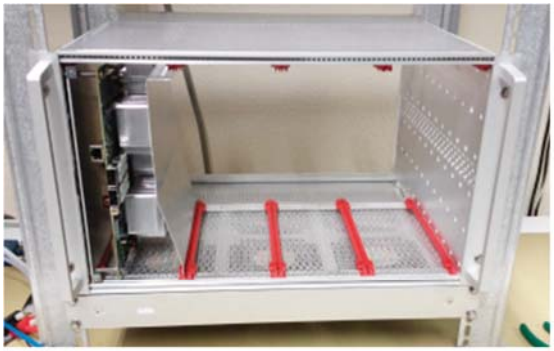
A summary of the comparison results is in Table 10 below.

Table 10. AAVS1 comparison of measured vs calculated temperatures.

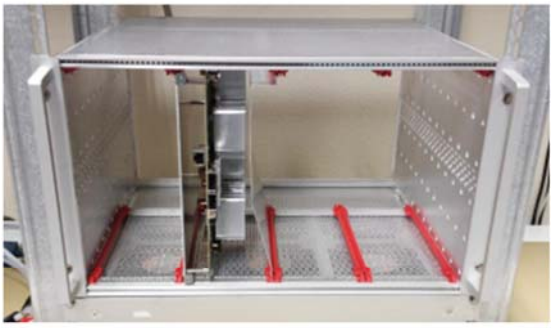
TPM Pos	**1**	**2**	**3**	**4**
Measured				
PCB Tempearure (°C)	*57.3*	*56.9*	*58.5*	*58.4*
Calculated				
PBC Temperature (°C)	61.4	57.2	56.3	58.5
% error	7.2%	0.5%	-3.8%	0.2%
Lower fans flowrate (m3/s)	0.138	0.144	0.143	0.143
Min ADC Temperature (°C)	71.6	68.4	69.6	70.2
Max ADC Temperature (°C)	79.9	77.0	77.1	78.8
Min FPGA Temperature (°C)	72.7	68.9	69.6	69.9
Max FPGA Temperature (°C)	76.5	73.4	72.7	74.9
HS channel - Air Temp. (°C)	30.6	31.8	30.1	33.6
HS channel - Air Speed (°C)	1.18	0.68	1.17	0.54

The differences in the measure and calculated temperature for the four TPM positions are +2.6%, +0.5%,-3.7% and +0.2%.

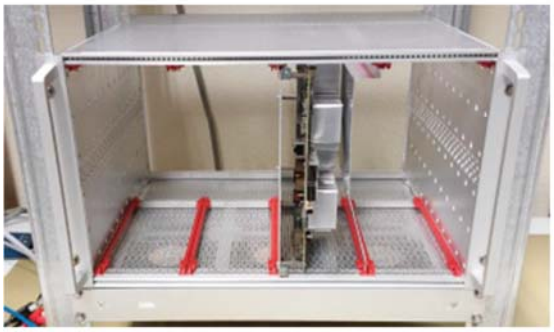
The agreement between measurement and simulation appears quite reasonable but it must be emphasized that the FPGA and ADC thermal dissipations are assumed values, and not measured.



T MAX (1): 57,3° C



T MAX (2): 56,9°



T MAX (3): 58,5°



T MAX (4): 58,4° C

Figure 87. INAF thermal test hardware.

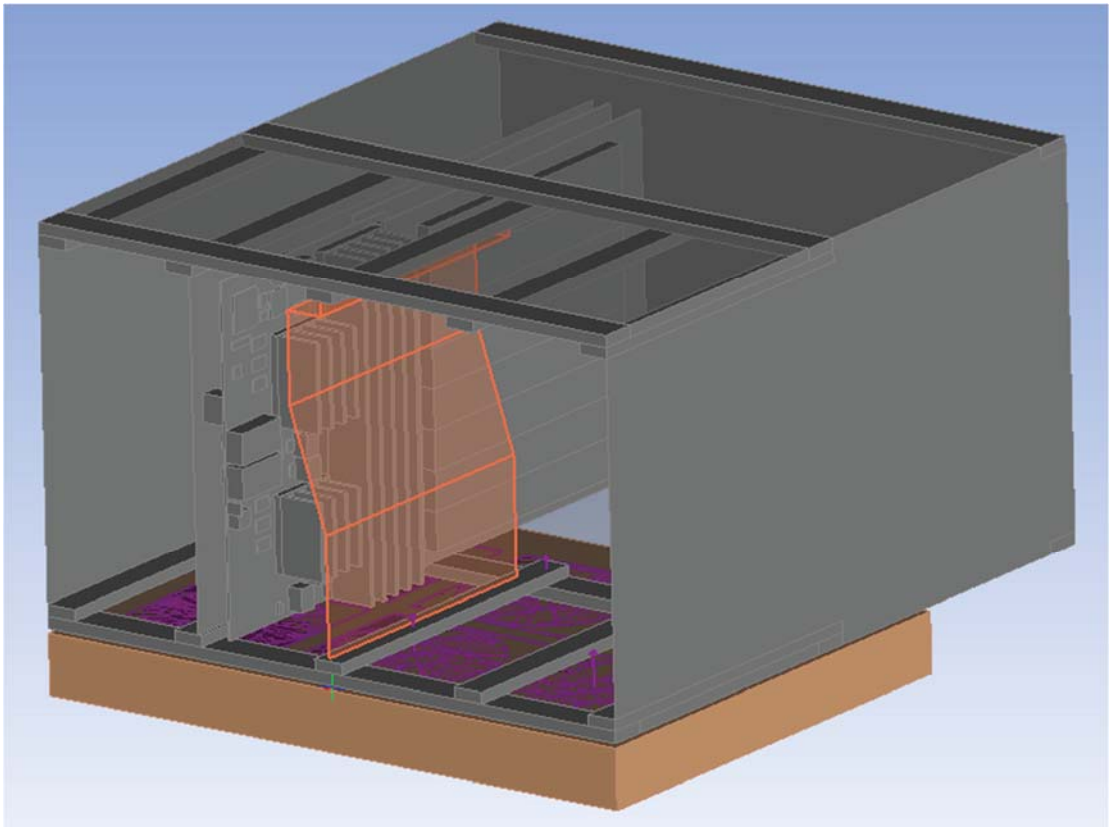


Figure 88. Thermal test model.

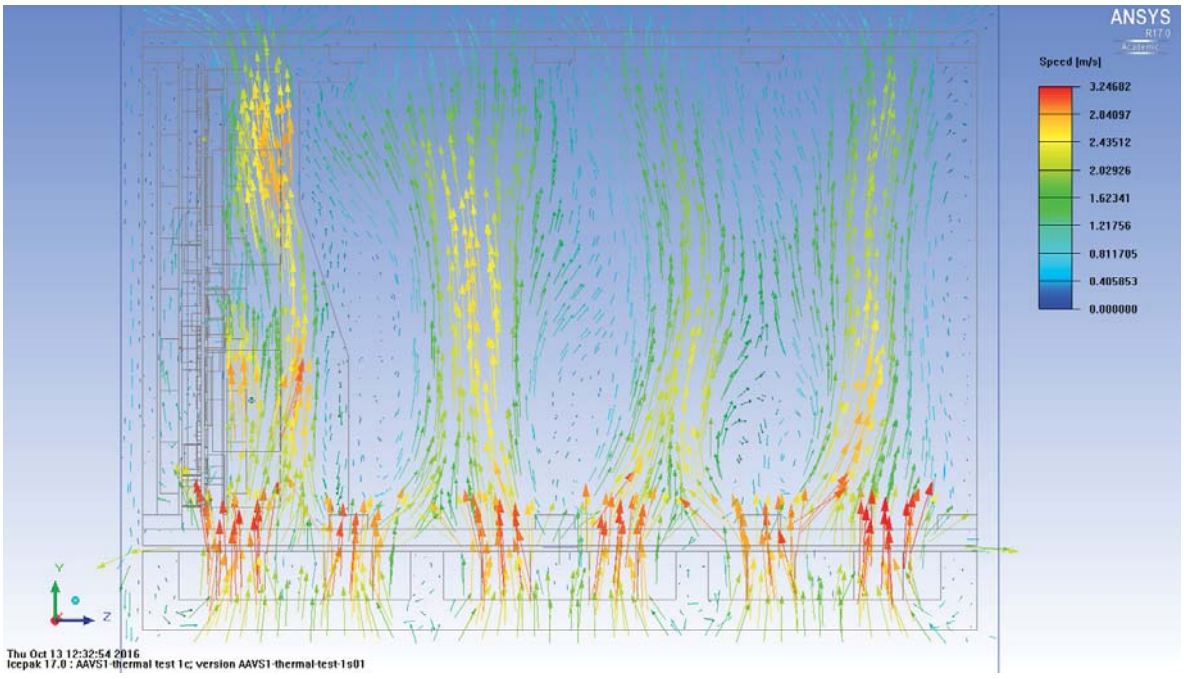


Figure 89. TPM position 1 air velocity.

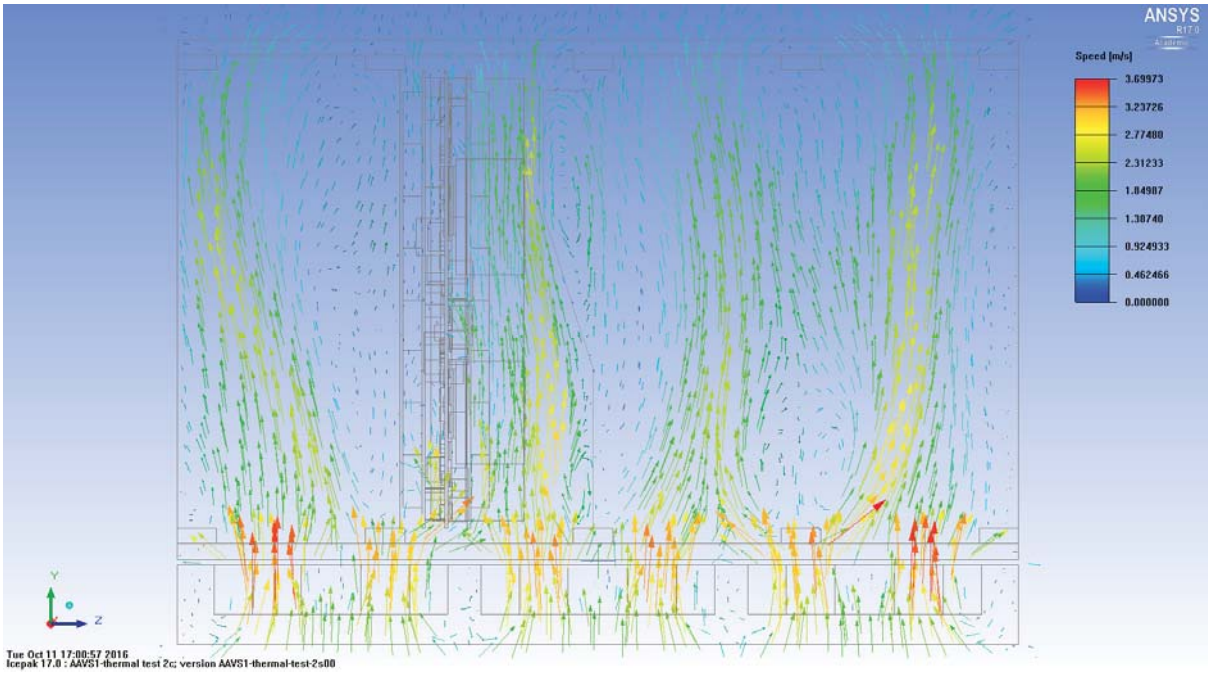


Figure 90. TPM position 2 air velocity

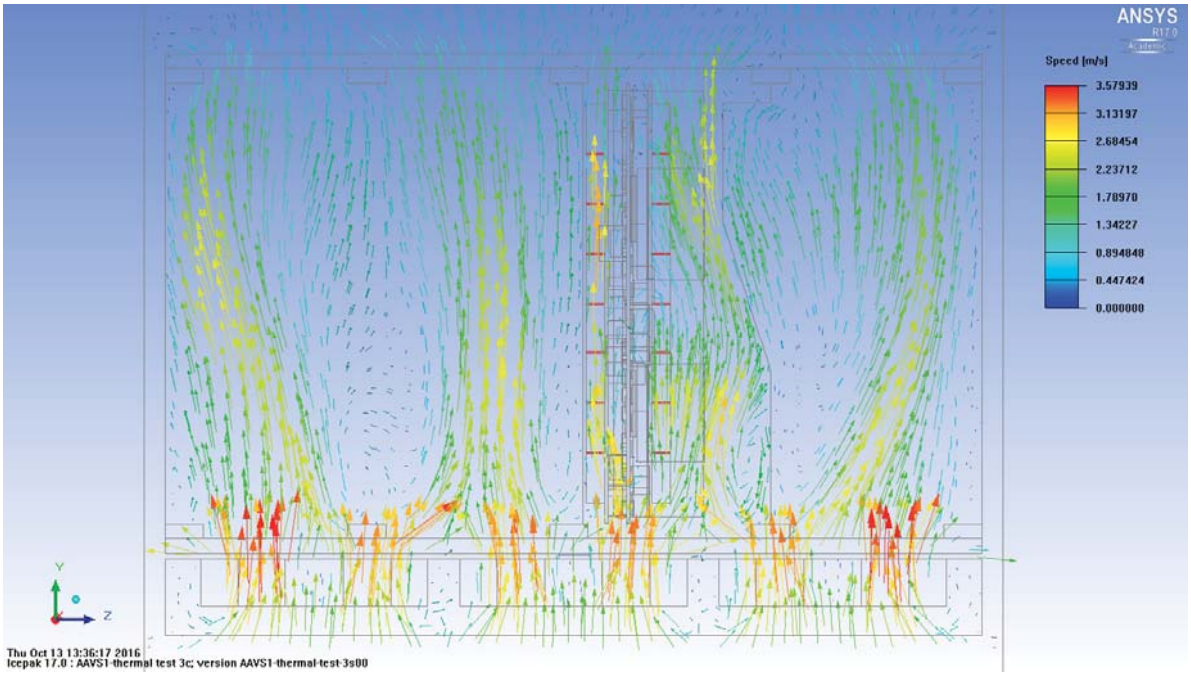


Figure 91. TPM position 3 air velocity.

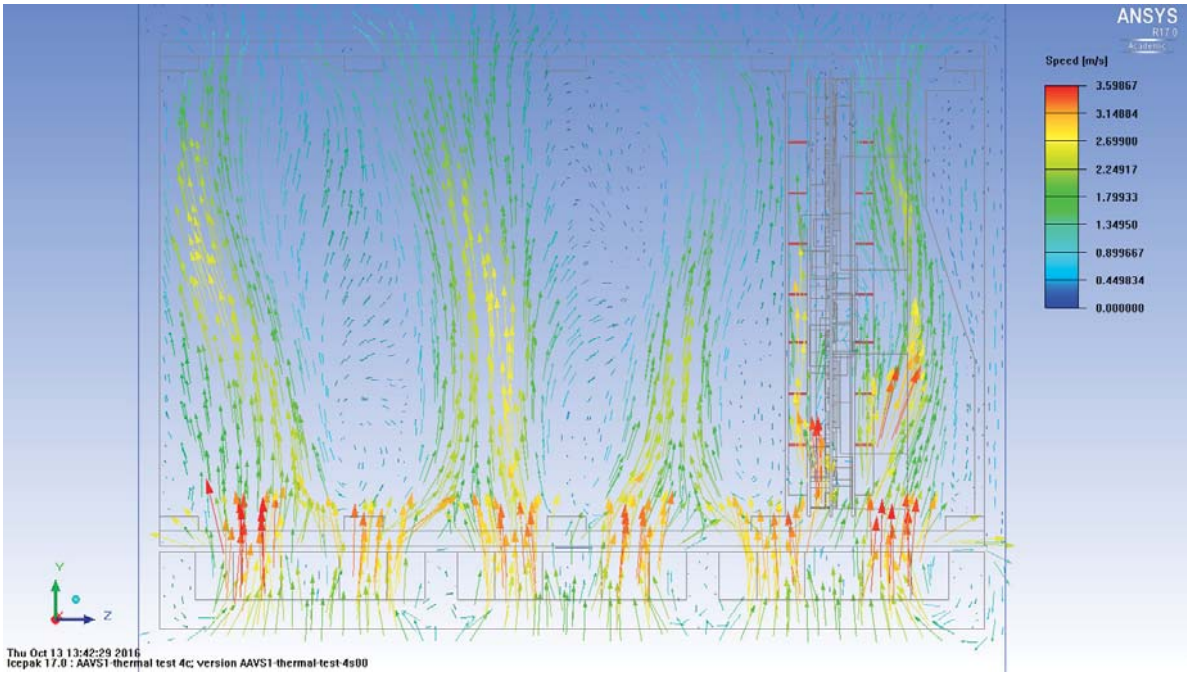


Figure 92. TPM position 4 air velocity.

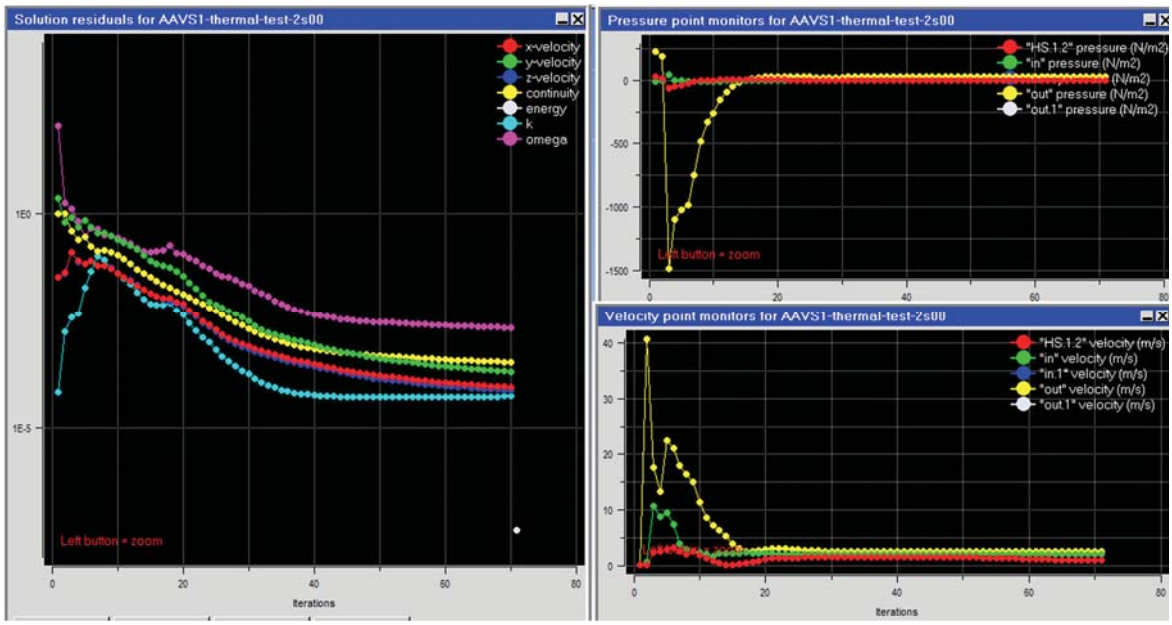


Figure 93. TPM position 2 simulation residuals and convergence monitors.

Figure 93 shows the solution monitor (pressure, velocity and temperature at chosen points and residuals for the flow parameters) for the thermal test simulation for TPM position 2. After 30 iterations the pressure and velocity at monitoring points above and below the fans and in one of the air channels are stable and after 70 iterations the solution residuals are acceptably small.

Initially small models such as the thermal test simulation were run on a desktop PC. To accelerate the solutions and to provide the required memory for a model of the complete cabinet they were later run on a server with 48 cores and 128 GB memory. Although this should allow faster solution, particularly important for large models, errors in the software when using parallel processing became apparent. An example, an AAVS1 sub-rack model (described in Section 4) is shown below in Table 11

and Figure 94. Similarly, the use of non-conformal meshing to reduce the mesh count and accelerate solution proved to be unreliable. ANSYS have acknowledged these problems and confirmed that their software engineers are investigating but there is no indication that the problem will be fixed in the near future. Accordingly, the simulations are being restricted to small problems (e.g. a ⅛th slice of an 8 TPM sub-rack) and run using the serial solver only. However it is possible to run a number of problems simultaneously on the server without being limited by memory or CPU.

Table 11. Comparison of serial and parallel solvers.

Model Lower fans flowrate (m3/s)	**AAVS1 6 fans** 0.115				**AAVS1 6 fans** 0.147			
TPM Pos	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**
PCB Temperature	78.6	80.8	81.8	86.5	138.2	128.4	127.5	143.7
Min ADC Temperature	97.7	92.2	94.8	92.7	140.8	132.2	137.6	135.0
Max ADC Temperature	112.6	110.9	111.2	112.3	171.3	170.4	169.4	171.5
Min FPGA Temperature	99.6	99.2	90.9	105.9	143.7	140.3	132.6	151.4
Max FPGA Temperature	104.3	105.0	97.4	105.9	160.9	159.9	150.1	171.1
HS channel - Air Temp.	31.5				105.9			
HS channel - Air Speed	0.87				0.08			
Solution time (hours)	46.8				12.8			
Version	AAVS1-sub-rack-6fan-03				AAVS1-sub-rack-6fan-04			
parallel processors	serial				8			

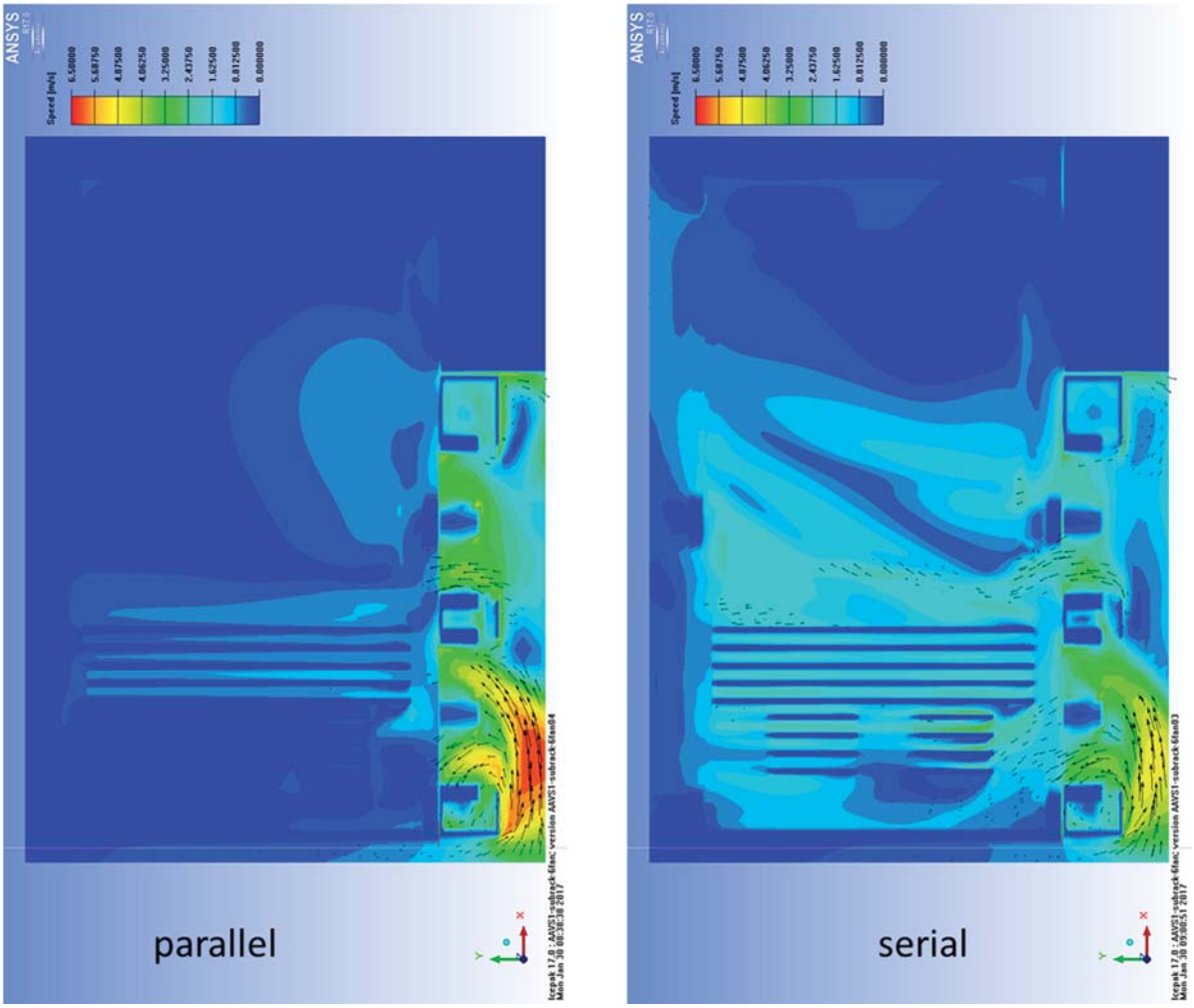


Figure 94. Air speed for parallel and serial solutions.

It is important to note the discontinuities in the parallel solution depicted in Figure 94.

5.4 AAVS1 cooling system design

5.4.1 Initial concept

A model based on the design of TPM sub-rack and 6-fan tray used for the thermal tests, with the addition of 2 air deflectors is shown in Figure 95 below. The FPGA and ADC thermal dissipations were set to 37.5W and 4.5W per device respectively to represent running firmware. This is 50% above the values used in the thermal test simulations. The inlet air temperature was set at 14°C which represents the installation in Pentair LHX20 cabinets on-site in Australia. This is 11°C below the values used in the thermal test simulations.

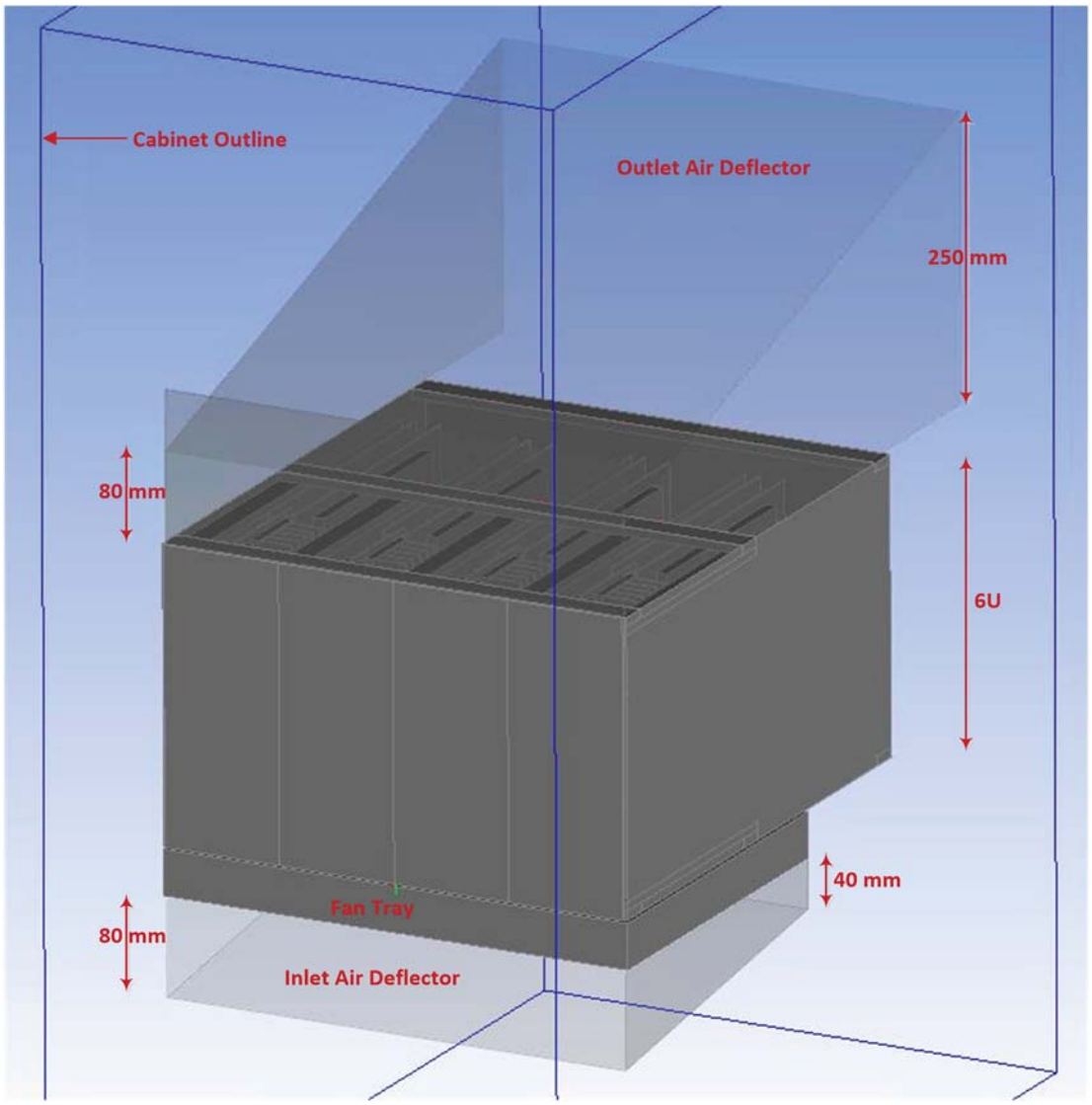


Figure 95. Initial AAVS1 thermal model.

The calculated PCB temperatures were between 69°C and 74°C compared to the values measured in the thermal tests of 57 to 58°C. The calculated junction temperatures are between 86°C and 95°C for the FPGAs and 80°C and 100°C for the ADCs. The required value is 70°C and therefore, taking into account the lower air inlet temperature, the temperature difference air-to-junction needs to be reduced by about 45%.

Figure 96 and Figure 97 below show the airflow through the sub-rack. The distribution between the TPMs is uneven and much of the flow avoids the heatsink. Figure 98 and Figure 99 show why this might occur.

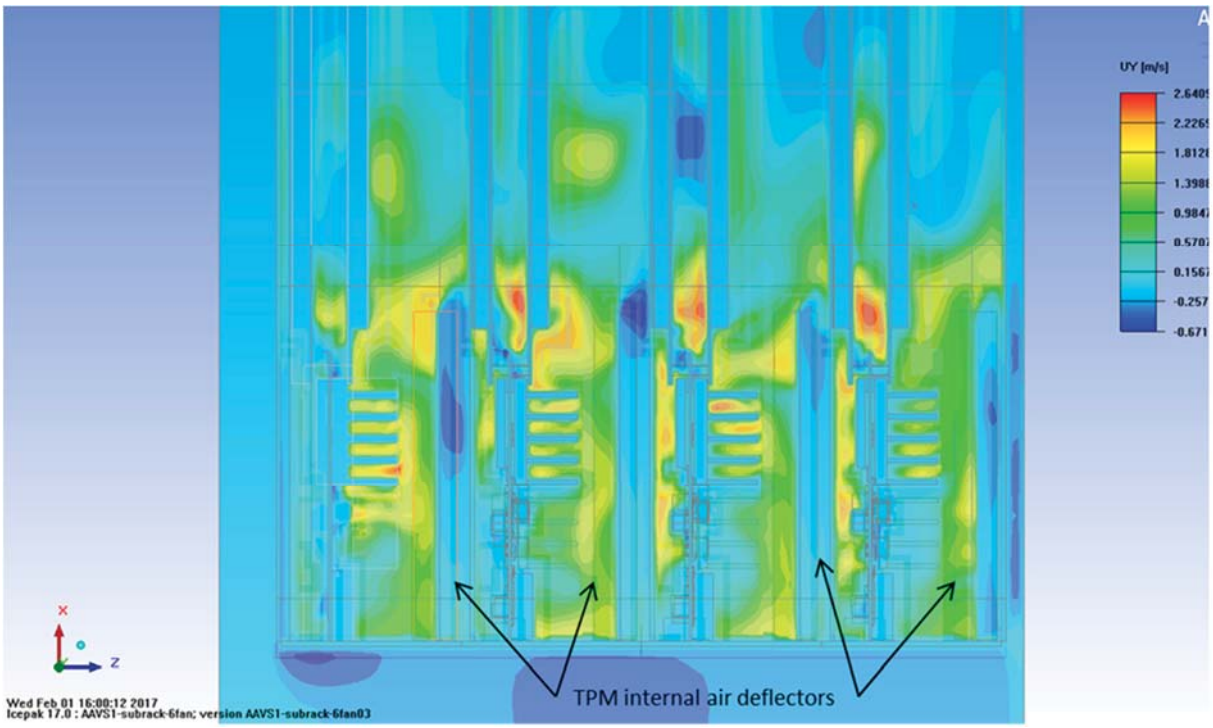


Figure 96. AAVS1 initial thermal model airflow, horizontal section.

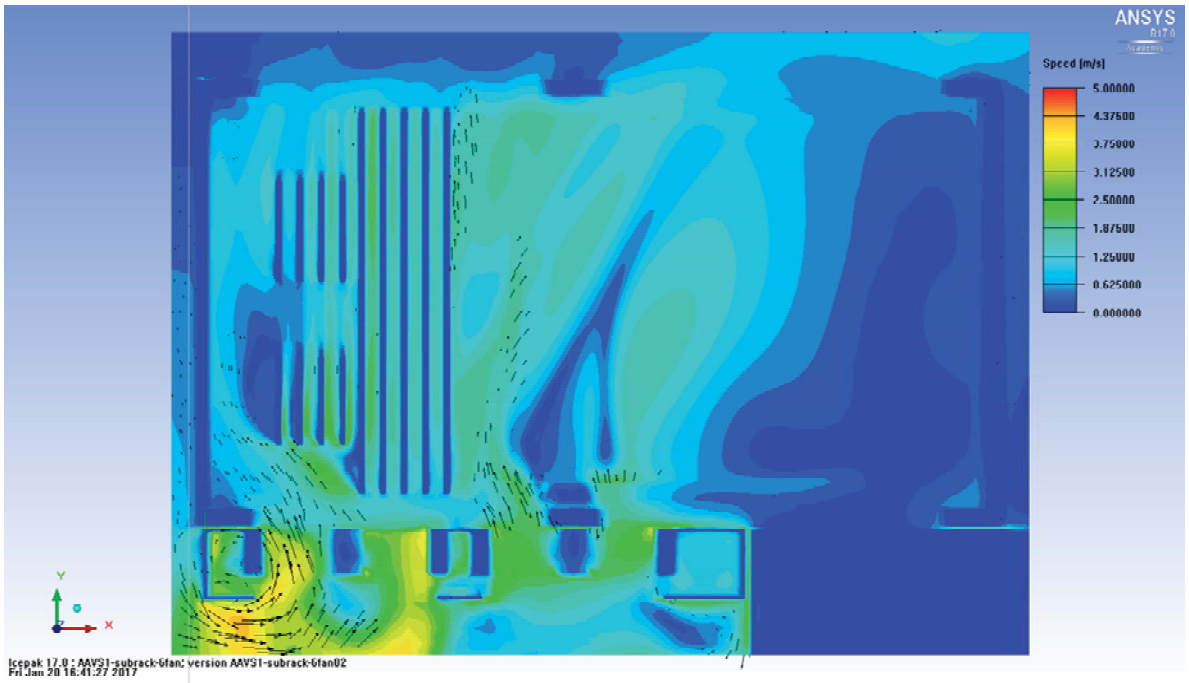


Figure 97. AAVS1 initial thermal model airflow, horizontal section.

The placement of the fans showed in Figure 98 resulted in an uneven airflow coverage over the heatsinks.

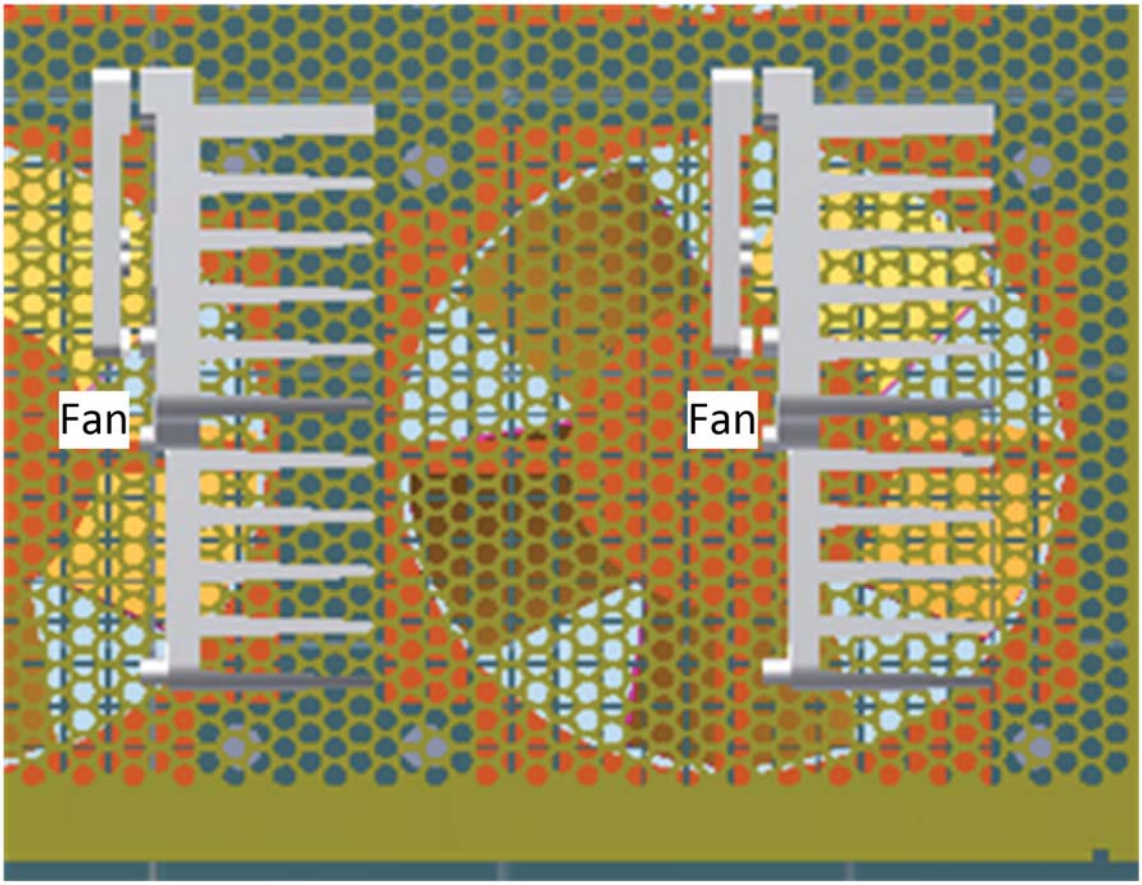


Figure 98. Fan positions.

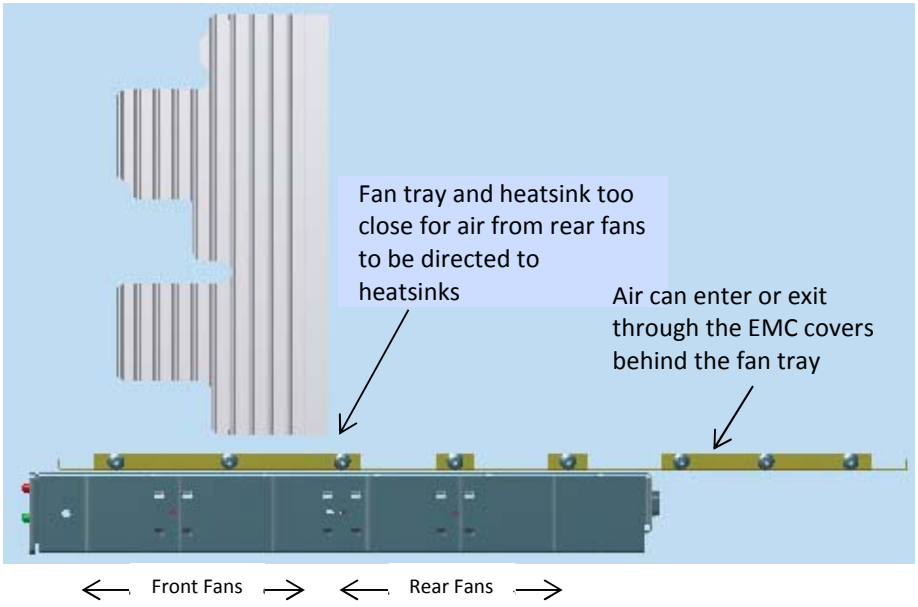


Figure 99. Design analysis.

5.4.2 Final design

To resolve the problems described above some simple additions can be made to the TPM sub-rack. This is shown in Figure 100 and Figure 101 below. Plena between the sub-rack and the fan trays allow air from the rear fans to be directed to the heatsinks and a generous 2U inlet and outlet units change the air-direction without excessive pressure loss.

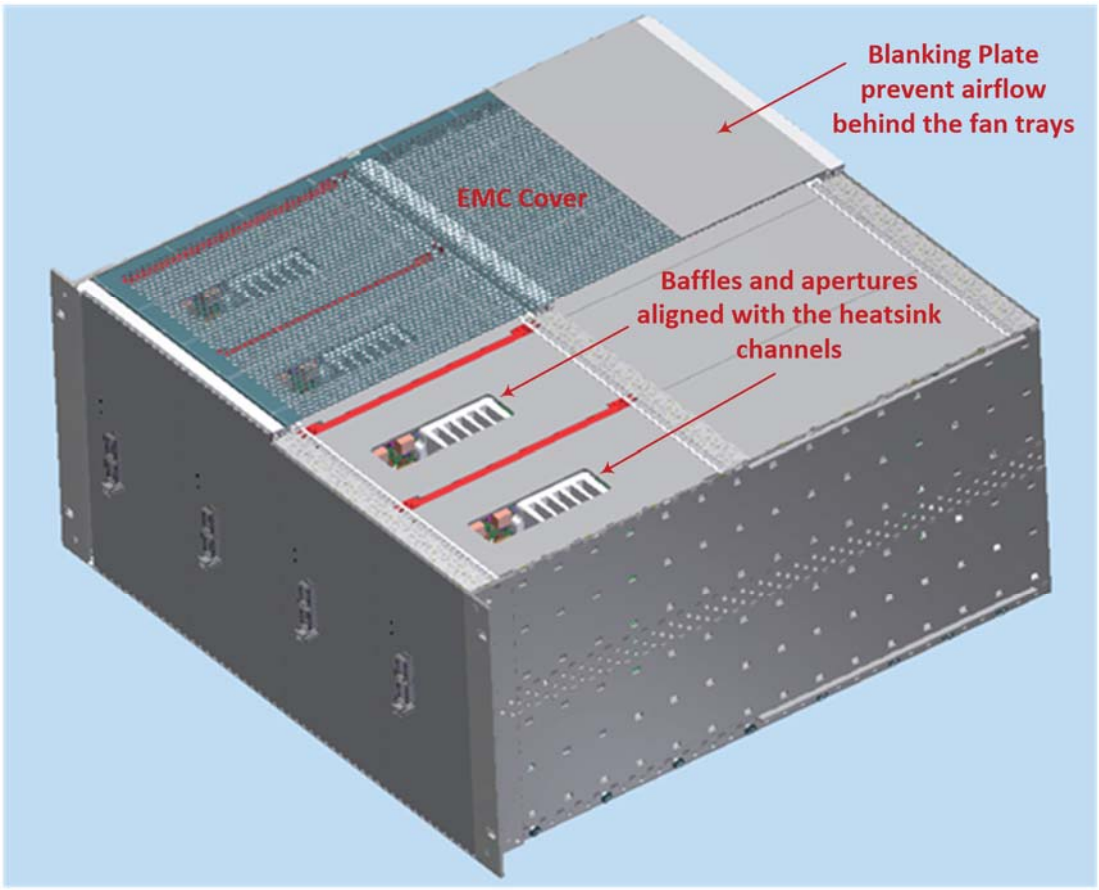


Figure 100. Cutaway (3/4 section) view of the AAVS1 TPM sub-rack.

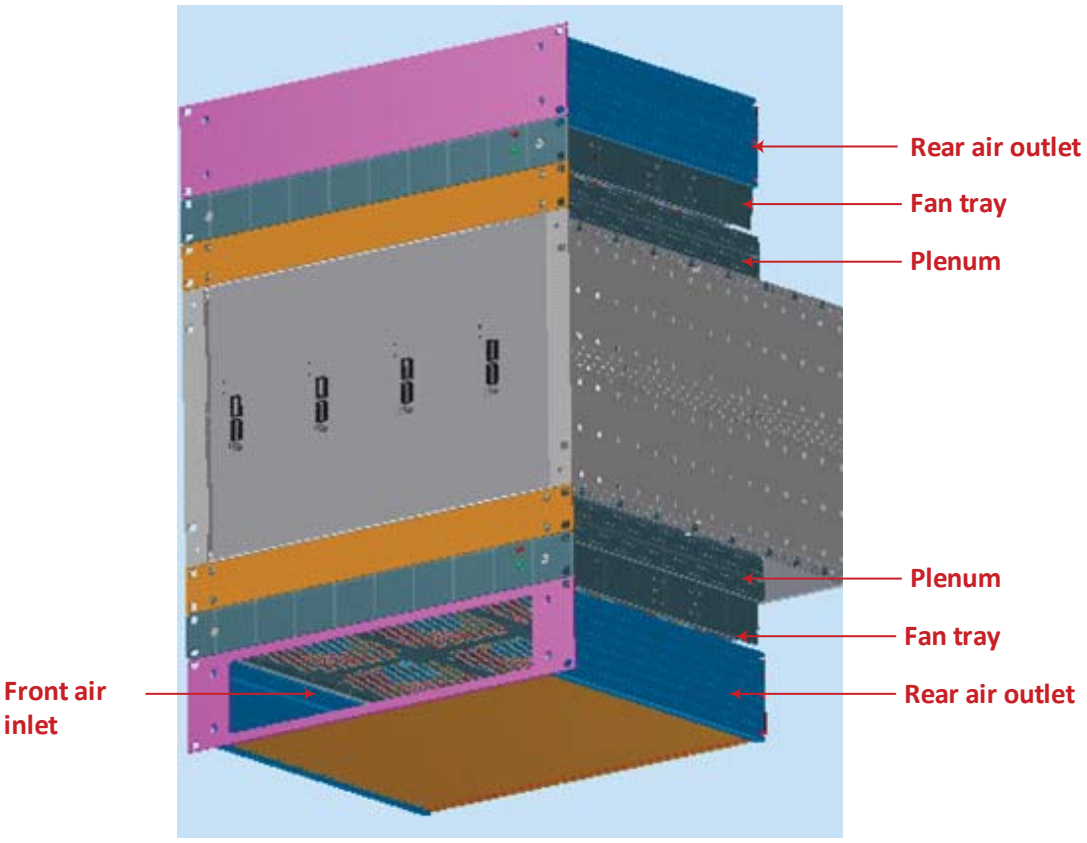


Figure 101. AAVS1 cooling design.

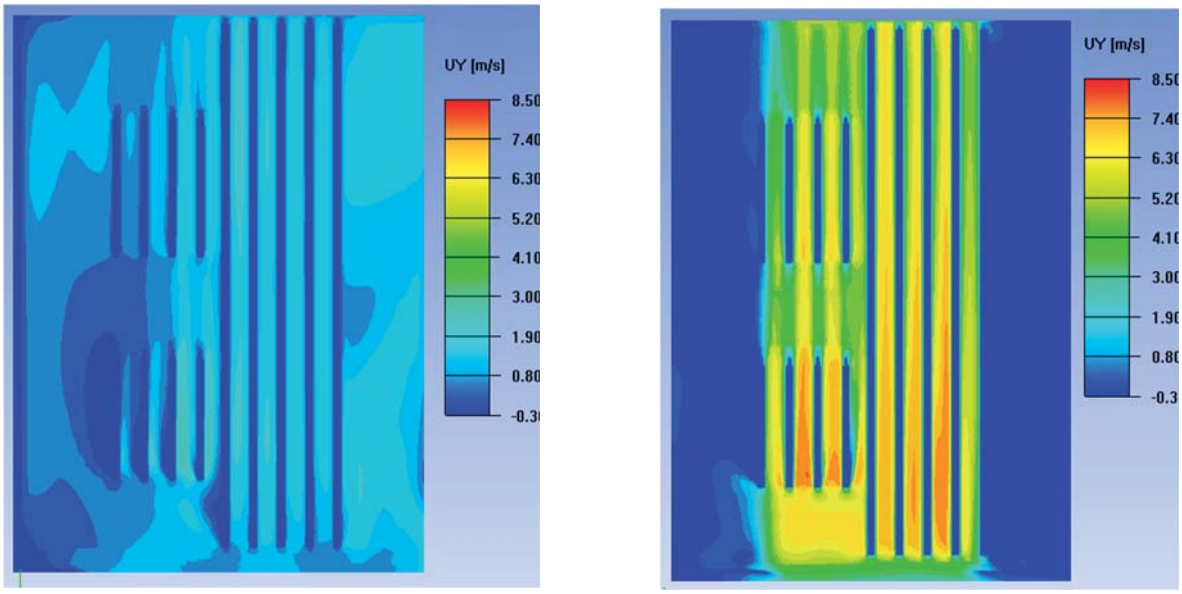


Figure 102. Vertical component of velocity through the heatsink for the initial and final designs. CFD model: AAVS1-sub-rack-6 fan unit (left). AAVS1-sub-rack-2 x 6 fans (right).

The same scale is used for both the plots in Figure 102.

Table 12. AAVS1 simulations for initial and final designs

Model	**6 fans and deflectors**				**2x6 fans, plena and baffles**			
Upper fans flowrate (m3/s)					0.105			
Lower fans flowrate (m3/s)	0.147				0.100			
Lower fans pressure rise (Pa)					38.8			
Upper fans pressure rise (Pa)	32.5				39.8			
TPM Pos	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**
pcb Tempearure	68.7	70.3	69.8	74.0	53.6	57.1	56.9	59.3
Min preADU Temperature	48.3				22.2			
Max preADU Temperature	70.8				45.0			
Min ADC Temperature	79.7				71.0			
Max ADC Temperature	100.0				81.2			
Min FPGA Temperature	92.0	86.8	85.9	88.0	74.7	72.2	72.0	71.9
Max FPGA Temperature	98.6	93.2	90.8	94.0	77.3	75.3	75.2	75.7
HS channel - Air Temp.	25.0				15.8			
HS channel - Air Speed	0.9				7.6			
Model/Version	AAVS1-subrack-6fan05				AAVS1-subrack-2x6fans00			

The enhancements to the airflow through the heatsink and the resulting temperatures are shown in Figure 102 and Table 12 respectively.

5.5 Configuration Management Artefacts

Configuration management of prototyping artefacts is as follows:
Software and firmware source files (and associated project or make files) are contained in SKA-TEL-LFAA-0500055- -LIS-1-LFAA Signal Processing Sub-system Reference Folder. This provides robust version control over the software and firmware prototyping work.

1. Documentation (including Design Specifications and Test Reports) are stored on Alfresco hosted by University of Cambridge.
1. Mechanical / thermal model source files are stored in SKA-TEL-LFAA-0500055- -LIS-1-LFAA Signal Processing Sub-system Reference Folder

Hardware design source files and manufacturing packages are stored in SKA-TEL-LFAA-0500055- -LIS-1-LFAA Signal Processing Sub-system Reference Folder.

5.6 Future Actions

The following prototyping work is expected to continue between June 2018 and LFAA CDR/ Bridging Phase, currently scheduled for December 2018.
The purpose of increasing the number of TPM boards in the LFAA cabinets and reducing power consumption is being pursued with the development of newer versions of both ADU and Pre-ADU boards.

In order to minimize cabling at cabinet level, a solution consisting of sub-rack management board and a backplane implementing connections among TPMs will be developed. This also allows for an easier installation/maintenance of the overall system.

5.6.1 Hardware

Hardware development and prototyping is expected to continue through 2018-2019 with the following priorities.

5.6.1.1 *TPM*

A more integrated version has been designed for LFAA (TPM 1.5) by INAF/Oxford in collaboration with Leonardo Finmeccanica, Sanitas EG and AAVID Thermalloy. Nowadays the process of optimization has not finished yet and a fine tuning of the design is still in progress and it will continue during the bridging phase.

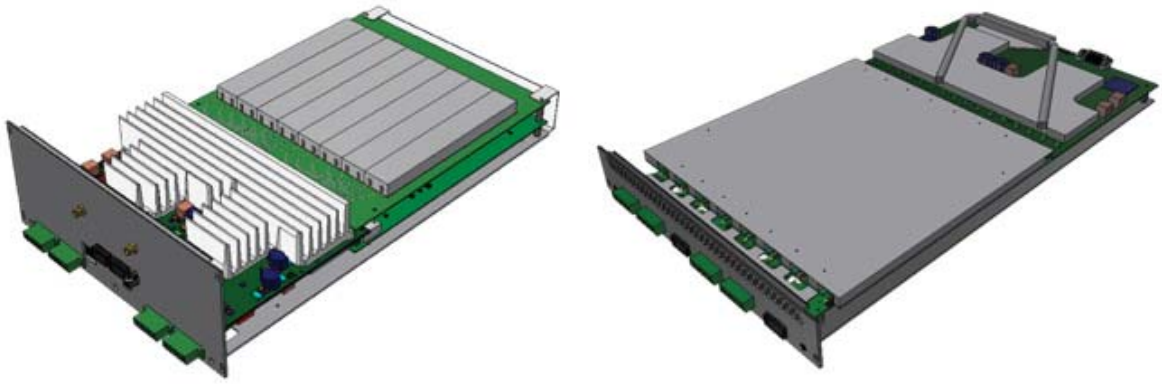


Figure 103. AAVS-1 TPM 1.2 (left) vs LFAA TPM 1.5 (right). The old heat sink of TPM 1.2 is replaced by a newer cooling system by liquid pipe.

5.6.1.2 *Pre-ADU*

The design of this board is still progressing simplifying the mechanics and interconnection to ADU, but also the RF electronics. In particular, the future generation of the board will employ a differential driver stage in front of ADC (what we called VGA). In this way, the last amplification stage and any digital control on board will be avoided because the VGA is directly controlled by SPI.

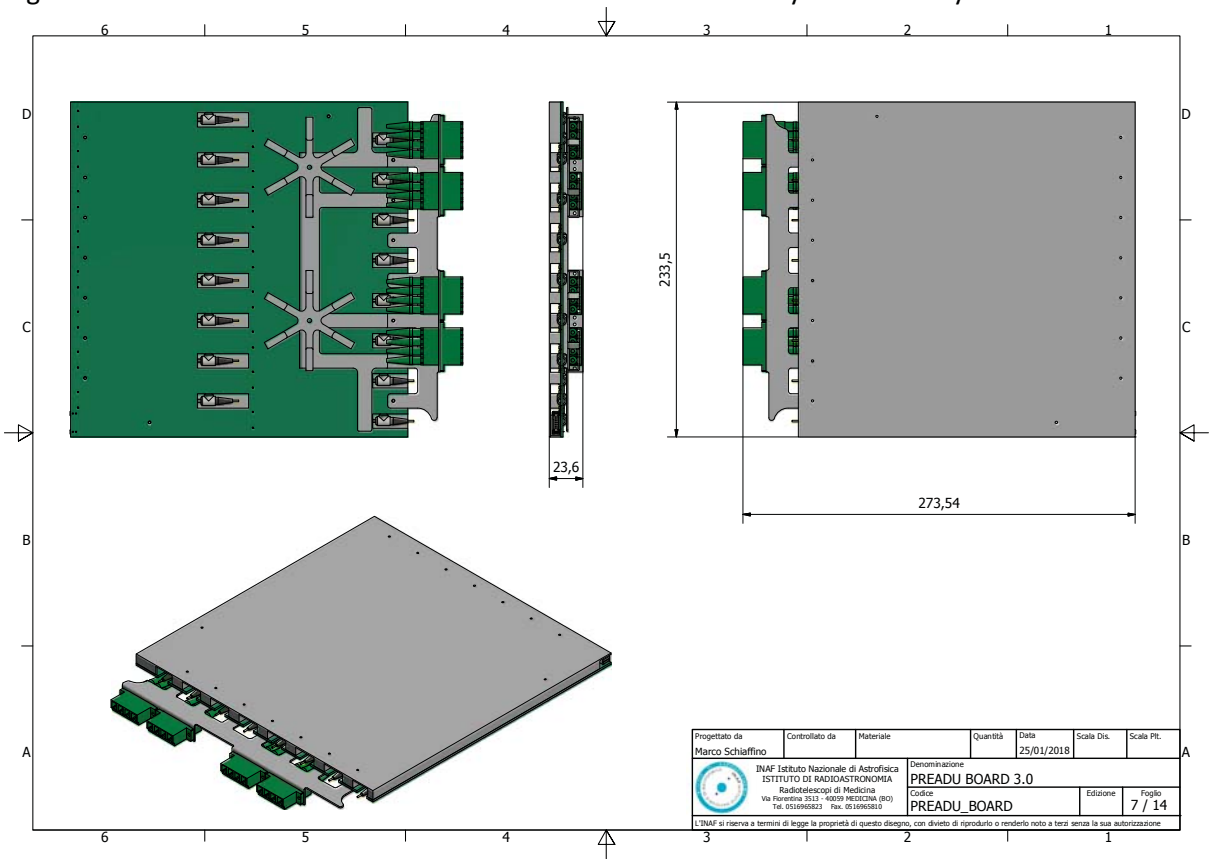


Figure 104. Picture of a new prototype Pre-ADU board.

The purpose of increasing the number of TPM boards in the LFAA cabinets and reducing power consumption is being pursued with the development of newer versions of both ADU and Pre-ADU boards.

In order to minimize cabling at cabinet level, a solution consisting of a backplane, implementing connections among TPMs will be developed. This also allows for an easier installation/maintenance of the overall system.

5.6.1.3 *ADU*

The main components of the ADU will be upgraded. The current FPGAs will be replaced by Xilinx 16 nm Kintex Ultrascale+ devices; the AD9680 ADCs will be substituted by AD9695 ADCs; DDR3L memories are going to be updated to the DDR4 family. The board will host sixteen memory chips, 8 Gbit each, with a 64-bit wide memory bus, for a total of 16 GByte memory.
Moreover, the bus between the two FPGAs will be implemented by using transceiver links, in place of previous normal LVDS lanes, allowing to double the data transfer rate.
Thanks to this evolution, the ADU board will maintain the original architecture, increase the performance/resources and reduce of about 20% the absorbed power.

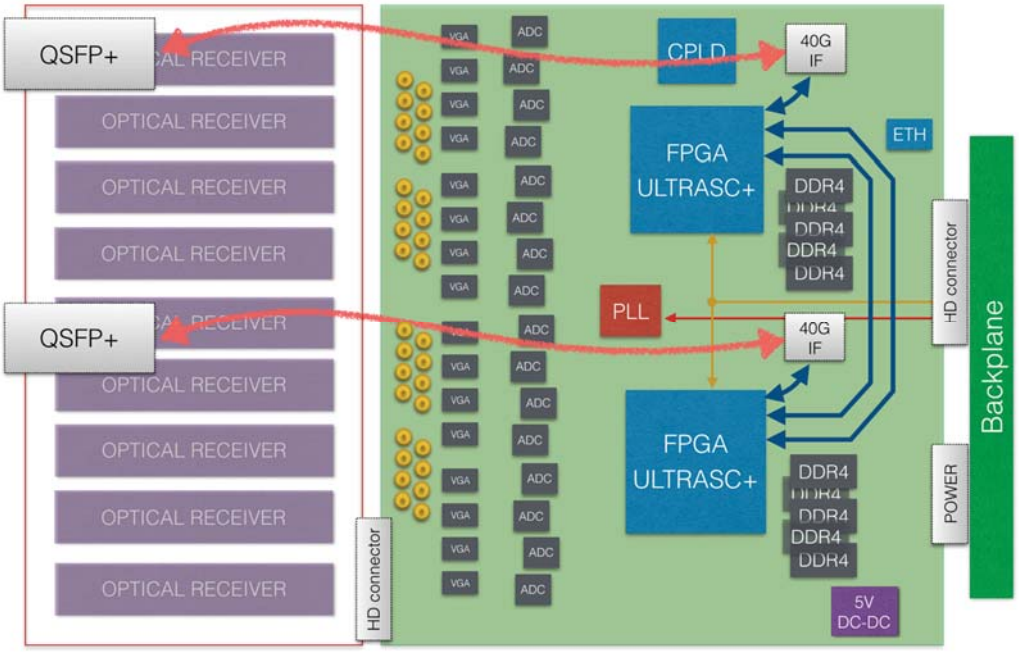


Figure 105. New ADU board layout.

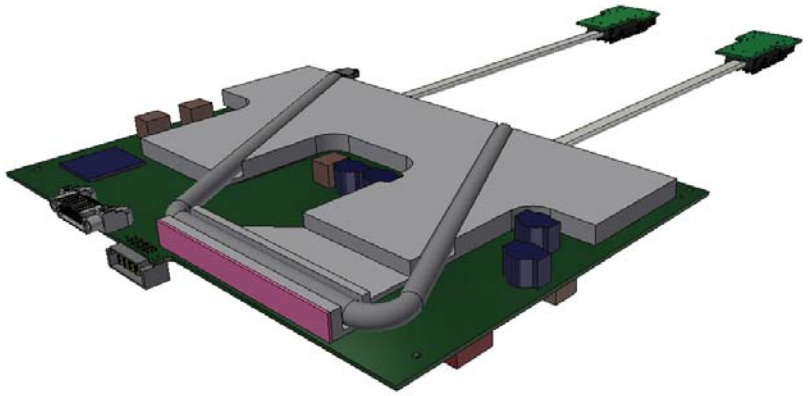


Figure 106. Picture of new prototype ADU board.

5.6.1.4 *Sub-rack and cabinet*

Specific sub-racks and cabinets will be designed for LFAA. Current proposed design is compatible with a standard chassis available on the market (eg, ABB customized by RGM mechanical company).

A preliminary schematic layout is shown in [RD16].

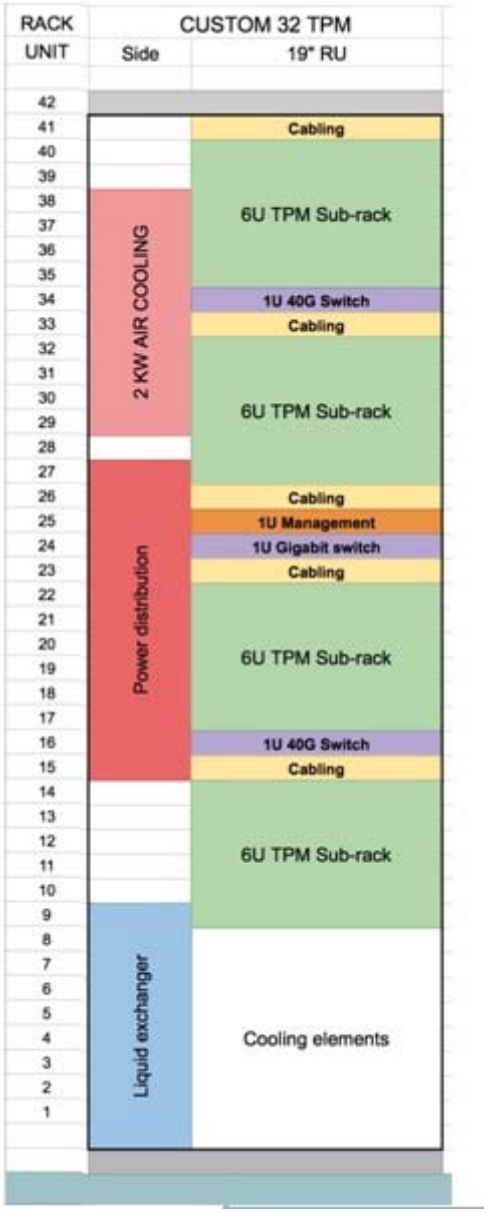


Figure 107. Cabinet preliminary layout front view.

The Power distributor element implements the general on/off switch, with manual activation and the required safety passive protections.

The power distribution unit manages all the controlled switches that can power all the other cabinet elements, with exception of the management board that shall be always powered.

The TPM sub-rack will be possibly coupled with the 40G Ethernet switch placed in the middle to implement a complete station module. With this approach the 40G QSFP connection are short and local and all the TPM of a single station are connected to the same switch to assure communication efficiency.

In the yellow cabling units there are empty space for fibers and general cabling to allow maintenance capability and to possibly extract a single TPM without other cable removal.
The cabinet management and the 1Gbit management switch (optional) can be placed in the middle or everywhere in the 19" column. The middle position can be optimal for clock cabling and network connections to each sub-rack.

The liquid cooling circuit is be placed on the bottom, with the liquid exchanger connected with the infrastructure liquid circuit by one side and to the cabinet internal circuit on the other. Also pumps and other liquid elements shall be placed on the bottom of the rack, with exception of the expansion vessel that shall be placed above the liquid circuit, to allow air removal and maintain the selected secondary pressure. A detailed description of the cooling sub-system can be found in [RD16].

The cabinet mechanics meets all the infrastructure specifications [AD16] in terms of occupied volume, maximum weight, available maintenance space, air and liquid floor interface, optical fiber interface from the top.

A possible cabinet complete design is presented. All the cabinet elements have been integrated with standard elements, where available, considering installation and maintenance processes.

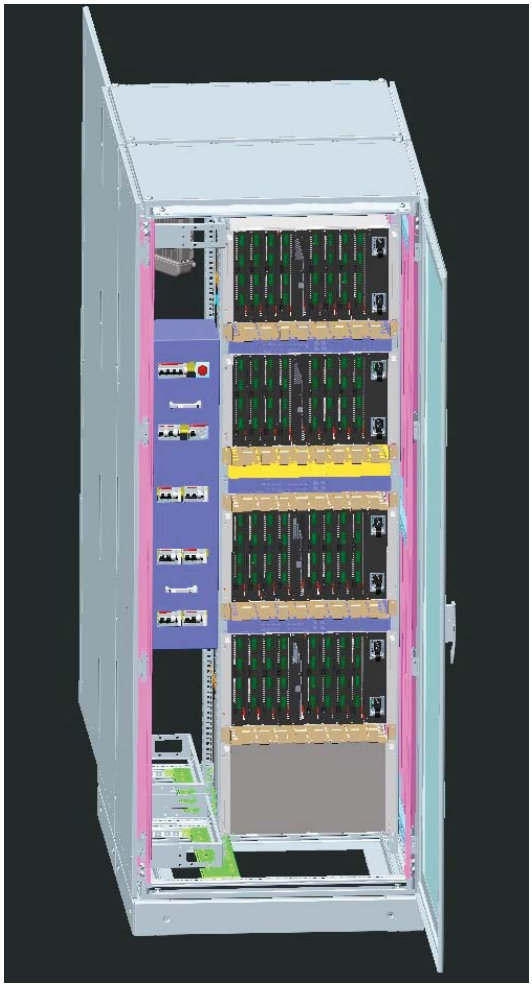


Figure 108. SKA LFAA TPM cabinet main elements.

The following prototyping work is expected to continue between June 2018 and LFAA CDR, currently scheduled for December 11th, 2018.

5.6.2 Signal Processing Firmware

The future work for firmware prototyping activities is expected to continue through 2018-2019, in parallel to the development and prototyping of the hardware. Main activities will mainly be focused to:

5.6.2.1 *Automation of diagnostic tests*

A number of diagnostic tests are already available in the current firmware. Software procedures to exploit these tests are in progress, and will require some tuning of the test cores in the firmware. The goal is to provide precise diagnostics on all the interfaces, validation of the firmware correct behaviour, and fault identification.
Work is relatively modest, and occurs in parallel to diagnostic software development.

5.6.2.3 *Transient buffer for antenna samples*

The possibility to store long sequences of antenna samples, as digitised in the ADCs, allows for a number of diagnostic tests. Samples can be analysed for missing codes, code uniformity and clock jitter. Samples can be processed in software and the result compared to the beamformed samples sent to the correlator. Some custom experiments (mainly cosmic ray observations using the induced EM pulse) require antenna data to be stored in a circular buffer, with trigger latency up to several 10 ms.
Currently an antenna sample buffer can be implemented in the firmware for a limited amount of time, using internal RAM blocks in the FPGA. Buffer size is limited to tens of microseconds, useful only for basic diagnostic tests, and occupies a significant amount of resources.
Using DDR memory, samples from up to 2 antennas per FPGA can be stored. Total DDR size allows for about 100 ms of buffer time.

5.6.2.4 *Support for new version of the TPM*

New revision of the TPM board (V1.5) uses a slightly different FPGA, with DDR4 memory (instead of DDR3), and serial FPGA-to-FPGA interface. Some re-adaptation of existing firmware will be required to operate it on the new board. In particular, some peripheral interfaces need to be changed in the new board, DDR addressing scheme must be revised for DDR4, and placement optimization in the polyphaser filterbank must be adapted to the internal layout of the FPGA.

5.6.2.5 *Support for 40 GB IP core in the station beamformer*

The current firmware uses the 40Gb Ethernet interface as 4 separate 10G channels. This is supported in the adopted network switch, but is not generally available in all commercial network switches. Separate 10G lanes have severe limitations in terms of bandwidth sharing among different lanes. A 40G MAC has been made available from Xilinx. The Ethernet and UDP core is being developed by RAL. This core will also manage ARP protocol which is not currently supported.
Using the interface as a full 40 Gb Ethernet also requires some adaptation of the station beamformer.

5.6.2.6 *Use of a single 40Gb interface per TPM*

The AAVS1 firmware uses both 40G interfaces on each ADU to transmit station beam data; it is foreseen to use one interface for the same task requiring only one Ethernet connection to the 40G. This requires moving data from one FPGA to the other using the high speed link connecting them, sharing the link with the tile beamformer. This requires the new interconnection between FPGAs in the TPM V1.5, and therefore this work will start after the previous point.

5.6.2.7 *Fast Transient Buffer formatter*

Fast Transient Buffer ECP requires that LFAA stores up to 900 seconds of beamformed data samples, requantised at 2 bits, for a total bandwidth of 150 MHz per station. Buffer will be implemented in MCCS. Firmware in SPS must requantise the samples for the required subset of frequency channels and stations, format them into SPEAD packets and send them to MCCS. Requantisation is dynamic, to reduce the quantisation losses.
This firmware will be included in the output section (SPEAD formatter for CSP packets) of the station beamformer.

5.6.2.7 *RFI detection*

Current RFI detection core is relatively simple, with fixed parameters. This is only partly compliant with the existing requirements. A more flexible core, providing programmable RFI detection timescale and thresholds, is required.

6 Residual Risks

6.1 Prototyping Residual Risks and Mitigation Plans

A complete list of SPS risks (including technical risks that were not actively prototyped during Pre-construction), along with mitigation / contingency plans, probabilities and severities can be found in the LFAA SPS Risk Register [RD1]. Some risks were retired by various activities for AAVS1, as described in Section 3.2.

Risks associated with LFAA SPS future developments are fully described in [AD2]. Risks associated to assumptions and design decisions are described in section 4.1 and 8 of that document, respectively. Furthermore, manufacturing risks are detailed in Section 14.1.5 of that document.

This section shows as an example a few open risks for the envisioned prototype activities from June 2018 and LFAA CDR/ Bridging Phase, currently scheduled for December 2018.

STATUS	RISK EVENT	RISK CAUSE	IMPACT/CONSEQUENCE	EXISTING MITIGATIONS	RISK RATING
Open	Clock distribution & PPS done with digital PLLs and PPS modulation inside clock	Lack of requirements	SPS does not work	Currently under evaluation, clock distribution redesign	***MEDIUM***
Open	FPGA software	The support of software tools for FPGAs is not be granted for the entire telescope operation period	Firmware programs cannot be updated or modified	Current version of all tools in the tool chain, including libraries, shall saved in one or more dedicated machines under configuration	***LOW***
Open	Single technology supplier	Suppliers stop the production of parts	Replacement or substitution of parts is not possible	Component production status monitoring, supplier agreement, volume purchase, board redesign	***LOW***
Open	Component obsolescence	Components get obsolete	Replacement or substitution of parts is not possible	Component production status monitoring, supplier agreement, volume purchase, board redesign	***LOW***
Open	Two stations for each cabinet	High integration	Difficult board handling	Accurate design for maintenance	***MEDIUM/LOW***
Open	Distributed AC-DC power supply	Commercial AC-DC power supply modules involved	Changing supplier	Find multiple power supply sources	***LOW***
Open	TPM cooling system by heat pipe technology	Design cost increase	Run out of budget	Prototype and verify production costs	***LOW***
Open	Backplane design integrated with cold plate design	Interface	Poor thermal transfer, mechanical contacts	Prototype and verify sub-rack integration	***MEDIUM/LOW***
Open	Clock distribution on the backplane	Possible interference with electrical signals	Interference noise on 10 MHz ref. clock	Layout separation and test clock quality	***MDIUM/LOW***

7 Conclusions

The AAVS1 prototyping and the experience gained during the design, production, testing and installation phases was effective for conceiving a new LFAA design.
The knowledge acquired allowed us to optimize those parts of the design that may lead to an easy assembly, integration and testing phases.
As mentioned in this document, the cabinet feasibility was studied only, while the production of the new ADU 1.5, Pre-ADU 2.5/2.6, Sub-rack/Cabinet Management Board and Sub-rack, has already started.
After highlighting the new risks in Section 6.1 , it is strongly suggested to proceed with the prototyping of the new SPS-LFAA system during the next "bridging" phase, to get more detailed information that would be useful for the final manufacturing.

8 Appendix A - Intellectual Property Declaration

The following pages provide the Intellectual Property declaration from Sanitas EG.

SKA Intellectual Property Rights (IPR) Notification Form

Please indicate your response to the listed requirements

Please use one form for each IPR you wish to notify

No	Requirement	Response
1	Description of technology or work in relation to which IPR is said to exist. *(Use continuation sheets if necessary.)* *(This should include a brief description of what the function of the technology is and of how such technology carries out that function.)*	Ethernet management and test interface, including Xilinx SMAP test interface. This IP allow the management, test and quality assurance of FPGA based complex design
2	Brief outline of the relevance of this technology or work for the SKA Project. *(Use continuation sheets if necessary.)* *(This should include the identification of the products in which the technology or work is used – reference to an item in the approved Product Breakdown Structure is required here)*	This IP allow to efficiently manage the large number of TPM remote FPGA base system and to estimate the contribute to the MTBF of the FPGA design

SKA Intellectual Property Rights (IPR) Notification Form

3	Details of any filings for patents, utility models, registered designs etc. made in respect of the technology or work. *(This should include the application number of the right, any publication number and the number of any granted right.)*	Patented, not renewed, in 2010
4	Date on which first filings for patents, utility models, registered designs etc. in respect of the technology or work were made.	About 2006, request for patent date
5	Location of patent/design or trade mark office in which first filing(s) for the IPR was/were made. *(This will be a national or international trade mark, patent or registered design office such as the EPO, OHIM, USPTO or a national office (e.g. the German national patent office).)*	Italy
6	Countries/Jurisdictions for which patent, utility model, registered design etc. protection is or has been sought.	Italy

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Author: W. Turner

SKA Intellectual Property Rights (IPR) Notification Form

7	Type of IPR. *(State whether patent, copyright, design right, registered design, utility model, design patent, semiconductor topography right, database right, confidentiality rights or rights in trademarks or other rights.)*	☐ Patent ☐ Copyright ☒ Design Rights ☐ Registered Design ☐ Utility Model ('Innovation patent') ☐ Design Patent ☐ Semiconductor topography rights ☐ Database rights ☐ Confidentiality rights (Trade Secrets) ☐ Trademarks ☐ Other rights
8	Date of creation of the technology or work in which the IPR is said to exist.	2006 and 2010 for ethernet extension
9	Date on which IPR is said to have come into effect and become enforceable. *(This will either be the date of grant for a registered IPR or the date of creation of a physical embodiment of the work in relation an unregistered IPR.)*	Design start
10	Date on which IPR is said to cease to have effect and become no longer enforceable.	Design and production ended
11	Is the IPR said to be Background IPR or Foreground IPR? *(These are as defined in the IP Policy)*	☒ Background IPR ☐ Foreground IPR ☐ N/A (Third Party IPR)
12	If the IPR is said to be Background IPR but was created after you became an SKA Contributor then please provide a brief explanation as to how it came to be created outside the SKA Project.	Created before

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SKA Intellectual Property Rights (IPR) Notification Form

13	Countries/jurisdictions in which IPR is said to have effect.	All
14	Identify any key requirements as to territory, exclusivity, field of use and exclusions from field of use, duration, necessary business relationships, etc., that you would likely seek to impose on any prospective licensee (including the SKAO). *(Please ensure that any terms that are to be imposed on the use of the IP in the SKA appear here explicitly.)*	na
15	Details of individual creators of the technology or work in relation to which IPR is said to exist. *(State the names and addresses of all those persons said to have created the technology or work. List no more than five persons.)*	Sanitas EG employee, Monica Alderighi Sergio d'angelo

SKA Intellectual Property Rights (IPR) Notification Form

16	Name of IPR owner.	Sanitas EG srl
17	Postal Address of IPR owner.	Viale Restelli 3, 20124, Milano (IT)
18	Contact Details for IPR owner. *(State the name, email address and telephone number of the contact person.)*	Sandro Pastore, sandro.pastore@sanitaseg.it, cell +39 320 0945069

19	Details of any licences of the IPR already granted to third parties. *(State the name of licensee, licensed activity, date and term of licence for the IPR being registered here.)*	Name of licensee: na Licensed application: na Date of commencement: na Term of licence: na
20	Deleted	
21	Details of any licences that are likely to be granted to third parties in respect of the IPR in the future. *(State the name of prospective licensee, licensed activity, likely date and term of licence.)*	Name of prospective licensee: na Licensed application: na Likely date of commencement: na Term of licence: na

SKA Intellectual Property Rights (IPR) Notification Form

22	Status of embodied IPR ('Third Party IPR') Permissions. *(State details of any known IPR not owned by you which use of this technology or work would be likely to infringe absent an appropriate licence. Details to include nature of the embodied IPR and details of the owner of that IPR together with details of any approaches made to the owner to obtain any necessary licence(s).)*	na
23	Author Record. *(State the name and job title of the person who created the record.)*	Sandro Pastore, Sanitas EG, CEO
24	Date of Record. *(State the date that this record was last updated.)*	23 November 2017
25	Signature.	

9 Appendix B - SPS Prototype Test Reports

Prototype Test Reports are stored in: SKA-TEL-LFAA-0500055- -LIS-1-LFAA Signal Processing Sub-system Reference Folder